2017 Spintronics Workshop on LSI

June 5, 2017, 19:00 – 21:35

Rihga Royal Hotel Kyoto, Shunju I (2F), Kyoto, Japan

General Information

The 2017 Spintronics Workshop on LSI will be held at Rihga Royal Hotel Kyoto in Kyoto, on June 5, 2017, in conjunction with the VLSI Symposium on Technology as a Satellite Workshop of the 2017 VLSI Symposia. The workshop will focus on spintronics-based LSI technologies for high performance and ultra low power systems. Papers on current status, prospects and the remaining challenges in this field will be presented from invited speakers. The workshop is sponsored by Center for Innovative Integrated Electronic Systems (CIES), and Center for Spintronics Integrated Systems (CSIS), Tohoku University.

Registration

The workshop fee is free of charge, but registration is required.
http://www.cies.tohoku.ac.jp/2017_Spintronics_WS/registration

Deadline of advanced registration: May 31, 2017

Program

19:00-19:05	Opening remarks: Tetsuo Endoh (Tohoku University, Workshop Program Chair)
19:05-19:35	Invited talk 1 Rajat Agarwal (Intel) Memory trends and challenges for Data Center usages
19:35-20:05	Invited talk 2 Seung H. Kang (Qualcomm) TBA
20:05-20:35	Invited talk 3 Danny Shum (GLOBALFOUNDRIES) CMOS-compatible eSTT-MRAM from development to Manufacture
20:35-21:05	Invited talk 4 Junghoon Bak (Samsung) Overview and prospects of STT-MRAM for embedded memory application
21:05-21:35	Invited talk 5 TBA (Tohoku University)

Program Chair Tetsuo Endoh (Tohoku Univ.)

Program Committee H. S. Philip Wong (IEEE Executive Committee Chair of 2017 Symposia on VLSI Technology and Circuits)
Tadahiro Kuroda (JSAP Executive Committee Chair of 2017 Symposia on VLSI Technology and Circuits)
Hideo Ohno (Tohoku Univ.)
Shoji Ikeda (Tohoku Univ.)
Takahiro Hanyu (Tohoku Univ.)
Masaaki Niwa (Tohoku Univ., JSAP Executive Committee Member of 2017 Symposia on VLSI Technology and Circuits)

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