2015 Spintronics Workshop on LSI

June 15, 2015, 19:00-22:10

Rihga Royal Hotel Kyoto, Suzaku I (2F), Kyoto, Japan

General Information

The 2015 Spintronics Workshop on LSI will be held at Rihga Royal Hotel Kyoto, on June 15, 2015, in conjunction with the VLSI Symposium on Technology as a Satellite Workshop of the 2015 VLSI Symposia. The workshop will focus on spintronics-based LSI technologies for high performance and ultra low power systems. Papers on current status, prospects and the remaining challenges in this field will be presented from invited speakers. The workshop is sponsored by Center for Innovative Integrated Electronic Systems (CIES), and Center for Spintronics Integrated Systems (CSIS), Tohoku University.

Registration

The workshop fee is free of charge, but registration is required. Download the registration form below and send it to e-mail: support-office@cies.tohoku.ac.jp
or fax: +81-22-796-3432.

«« Click here for registration form.
Deadline: June 12, 2015

Program

19:00-19:15	**Opening Remarks: Tetsuo Endoh (Tohoku University, Program Chair)**	
19:15-19:40	Invited talk 1 **Gwan-Hyeob Koh (Samsung Electronics)** Issues of STT-MRAM Development	Chair: Hideo Ohno
19:40-20:05	Invited talk 2 **Hideo Sato (Tohoku University)** Properties of CoFeB-MgO Magnetic Tunnel Junctions with Perpendicular Easy Axis for Spintronics Based VLSI Applications	
20:05-20:30	Invited talk 3 **Akihisa Sekiguchi (Tokyo Electron)** STT-MRAM Market Perspective and Process Technology Update	
20:30-20:55	Invited talk 4 **Seung Kang (Qualcomm)** Redefining Embedded Nonvolatile Memory Use Cases: Harvesting STT-MRAM Performance and Endurance for Wearables and Internet-of-Things	Chair: Tetsuo Endoh
20:55-21:20	Invited talk 5 **An Chen (GLOBALFOUNDRIES)** Analysis of STTRAM Scaling and the Feasibility of High-Density Designs	
21:20-21:45	Invited talk 6 **Christophe Layer (CEA-Spintec)** Low-Power Hybrid STT/CMOS System-on-Chip Design Embedding Non-Volatile Magnetic Memory Blocks	
21:45-22:10	Invited talk 7 **Takahiro Hanyu (Tohoku University)** Challenge of MOS/MTJ-Hybrid Integrated Circuits Based on Non-Volatile Logic-in-Memory Architecture	

Program Chair Tetsuo Endoh (Tohoku Univ.)

Program Committee H. S. Philip Wong (IEEE Executive Committee Chair of 2015 Symposia on VLSI Technology and Circuits)
Tadahiro Kuroda (JSAP Executive Committee Chair of 2015 Symposia on VLSI Technology and Circuits)
Hideo Ohno (Tohoku Univ.)
Takahiro Hanyu (Tohoku Univ.)
Masaaki Niwa (Tohoku Univ., JSAP Executive Committee Member of 2015 Symposia on VLSI Technology and Circuits)

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