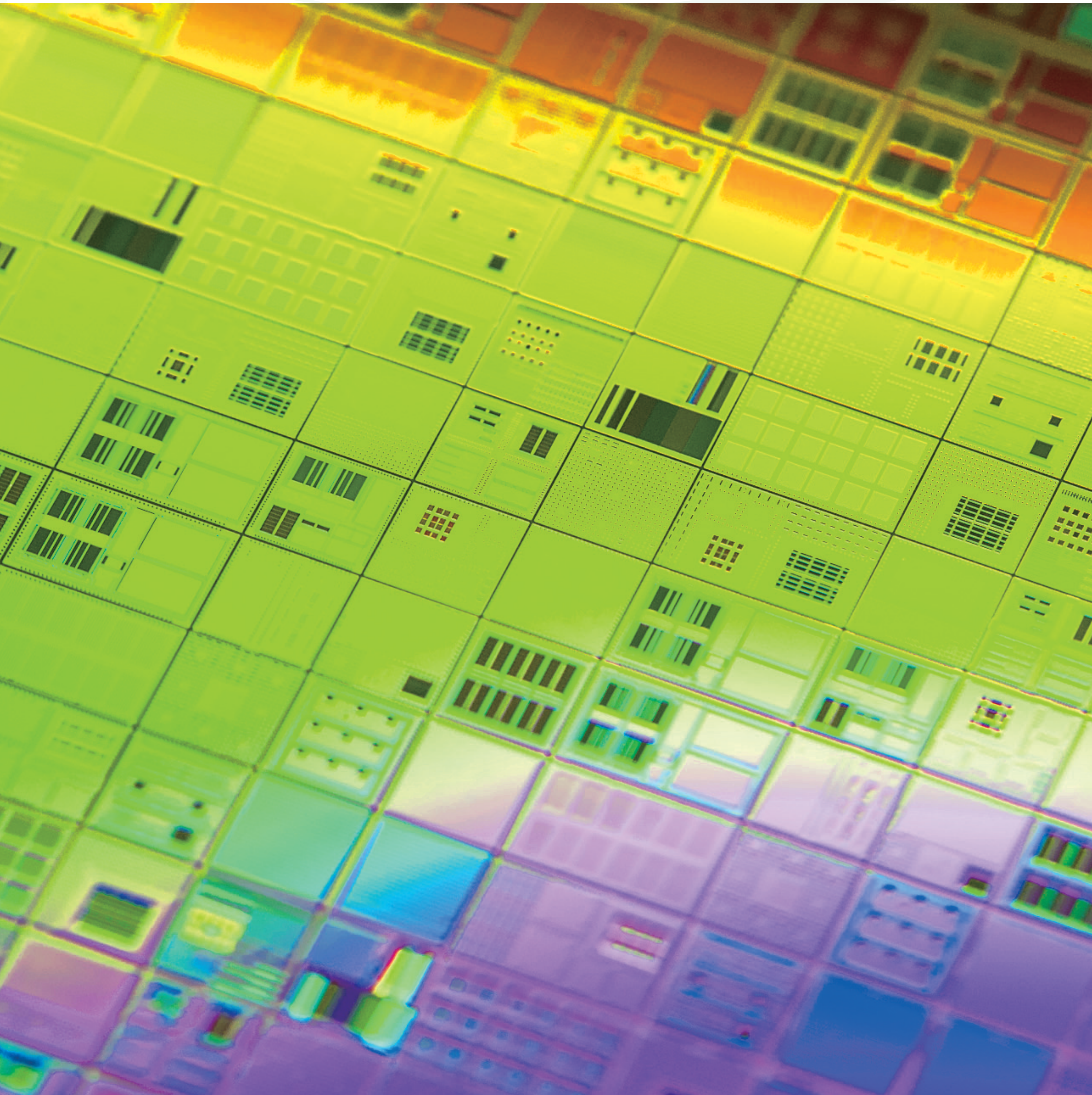
2025 EDITION

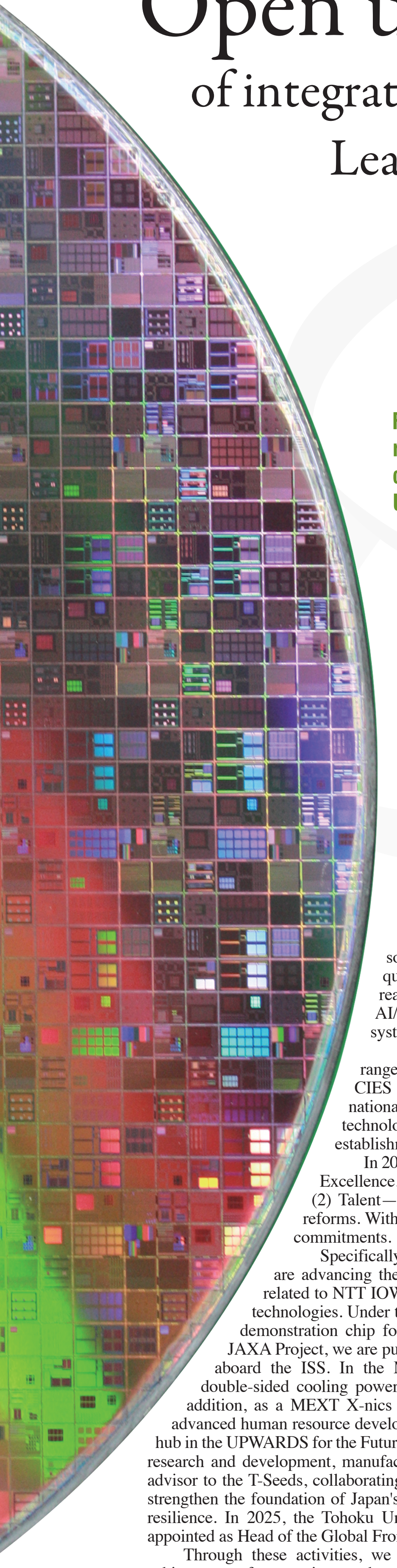
東北大学 国際集積エレクトロニクス研究開発センター

Tohoku University Center for Innovative Integrated Electronic Systems

TOHOKU UNIVERSITY

cies





Open up Innovation

of integrated electronics from the international industry-academic alliance!

Lead the recovery and new creation　　Leap toward world-class

feature Hardware

First privately donated research and development center by founded Tohoku University in Science Park

300mm wafer process line, facilities for device, characterization & physical analysis in university campus for the first time in Japan

*1 Official support from Miyagi Prefecture through the system of special zones for the promotion of private investment (information service related industries) that was applied for jointly by the Miyagi prefectural government and municipal governments in the prefecture.

*2 Official support from Sendai City through an amount corresponding to the fixed property tax, etc., according to an agreement made by Tohoku University and Sendai City.

Our Mission and Vision

The Center aims to contribute to the enhancement of global competitiveness in the field of next-generation integrated electronics systems, and work toward the creation of practical applications and new industries, through the research and development of innovative devices and its integrated electronic systems and constructing a consortium for this field under the international collaboration among industries, universities and government.

feature Software

Flexible joint research frame work between industry-academic alliance

Knowledge based on accomplishments between academic-industrial collaborations

Centralized administrative control and strategic operation of world-class intellectual properties of core technologies

Global standard joint research contracts

feature Core technology

Advanced core technologies and intellectual properties from materials/devices/ processes to system/architectures, created and reserved at Tohoku University under its "Research First" principle and "Open Doors" philosophy, and "Practice-Oriented Research and Education" ethos.

- Materials technology
- Device technology
- Fabrication technology
- Circuit design technology
- System design technology
- Software technology
- Algorithm technology
- etc.

Integrated electronics underpin virtually all industrial products and social infrastructure, and constitute a core technology that determines the quality of our daily lives. In response to global-scale demands such as the realization of carbon neutrality by 2050 and the advancement of an AI/DX-driven society, there is a strong need for innovative integrated electronic systems capable of achieving dramatic improvements in energy efficiency.

The Center for Innovative Integrated Electronics (CIES), in collaboration with a wide range of domestic and international companies as well as local governments, operates the CIES Consortium, which comprises industry–academia collaborative research, large-scale national projects, and regional collaboration projects spanning materials, devices, integration technologies, circuits, architectures, and systems. This year marks the 14th anniversary of its establishment.

In 2024, our university became the first institution to be certified as an International Research Excellence, committing to three core principles: (1) Impact—Creating social value for the future; (2) Talent—Fostering brilliant talent for the future; and (3) Change—Governance to accelerate reforms. With semiconductors as its primary domain, our Center contributes comprehensively to all commitments.

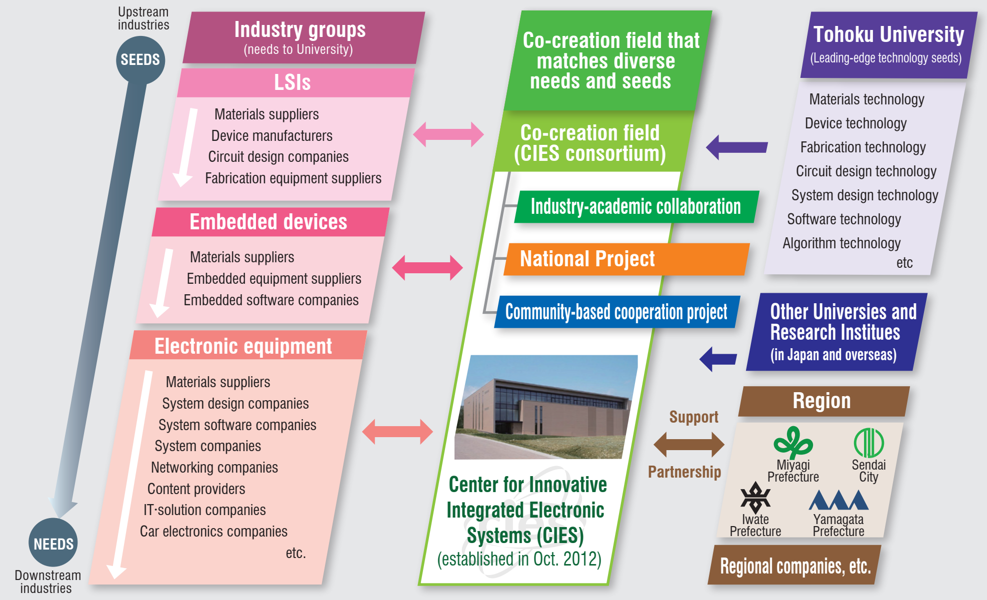
Specifically, in addition to international industry–academia research and development activities, we are advancing the development of wide-bandwidth buffer memory under the NEDO Post-5G Project related to NTT IOWN initiative, focusing on Photonics-electronic convergence interface memory module technologies. Under the NEDO AI Semiconductor Project, we have successfully developed the world's first demonstration chip for edge AI utilizing CMOS/spintronics hybrid technology. Furthermore, through the JAXA Project, we are pursuing demonstrations of standby-power-free systems and resistance to space radiation aboard the ISS. In the MEXT Power Electronics Project, we have successfully developed ultra-compact double-sided cooling power modules, thereby further advancing core technologies in integrated electronics. In addition, as a MEXT X-nics project "Innovative spintronics X semiconductor research hub"—we are promoting advanced human resource development in collaboration with 14 universities across Japan. We also participate as a core hub in the UPWARDS for the Future, working with industry and universities in both countries on innovative semiconductor research and development, manufacturing, supply chains, and human resource development. Moreover, we serve as an advisor to the T-Seeds, collaborating with industry, universities, colleges of technology, and government organizations to strengthen the foundation of Japan's semiconductor-related industries, foster human resources, and enhance supply chain resilience. In 2025, the Tohoku University Semiconductor Creativity Hub (S-Hub) was established, and I have been appointed as Head of the Global Frontier Human Resource Development Division.

Through these activities, we are committed to contributing to the realization of a carbon-neutral society, the achievement of economic growth and economic security, and the development of advanced human resources who will lead these efforts.

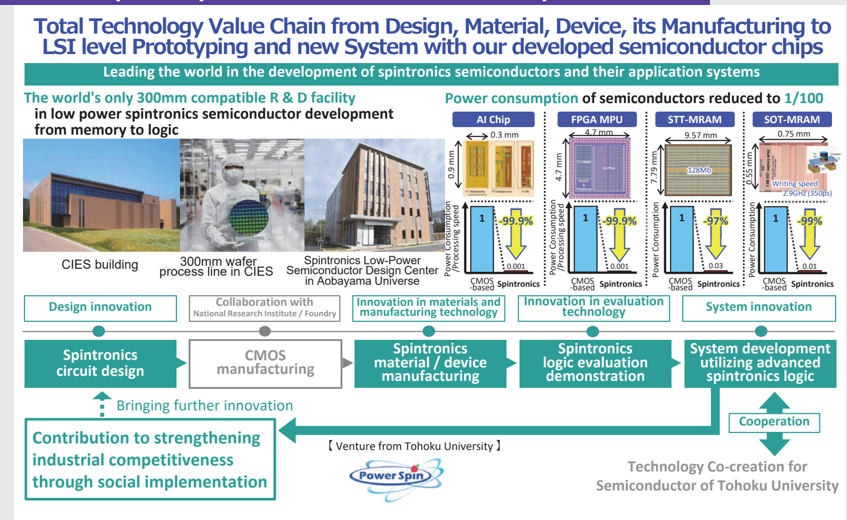
The growth and success of our Center to date would not have been possible without the continued support and cooperation of many stakeholders. We would like to express our sincere gratitude and respectfully ask for your continued support.

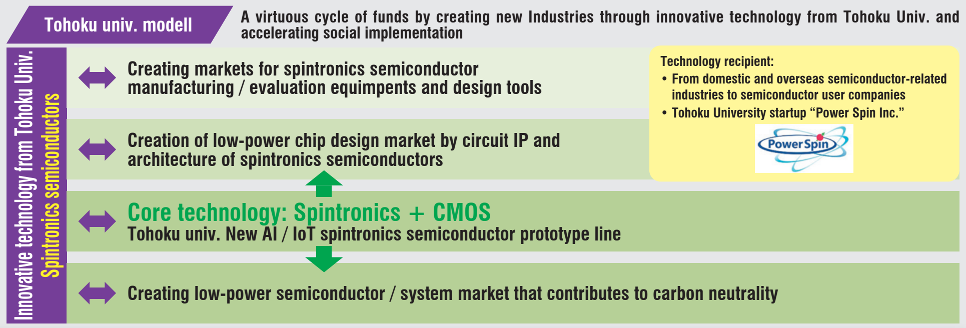
March 2026
Tetsuo Endoh
Director of CIES

Goal of the center : Model "B-U-B (Business-University-Business)"



Ultra-low power spintronics semiconductor development hub





CIES symbol and its messages

cies Center for Innovative Integrated Electronic Systems

Symbolic messages

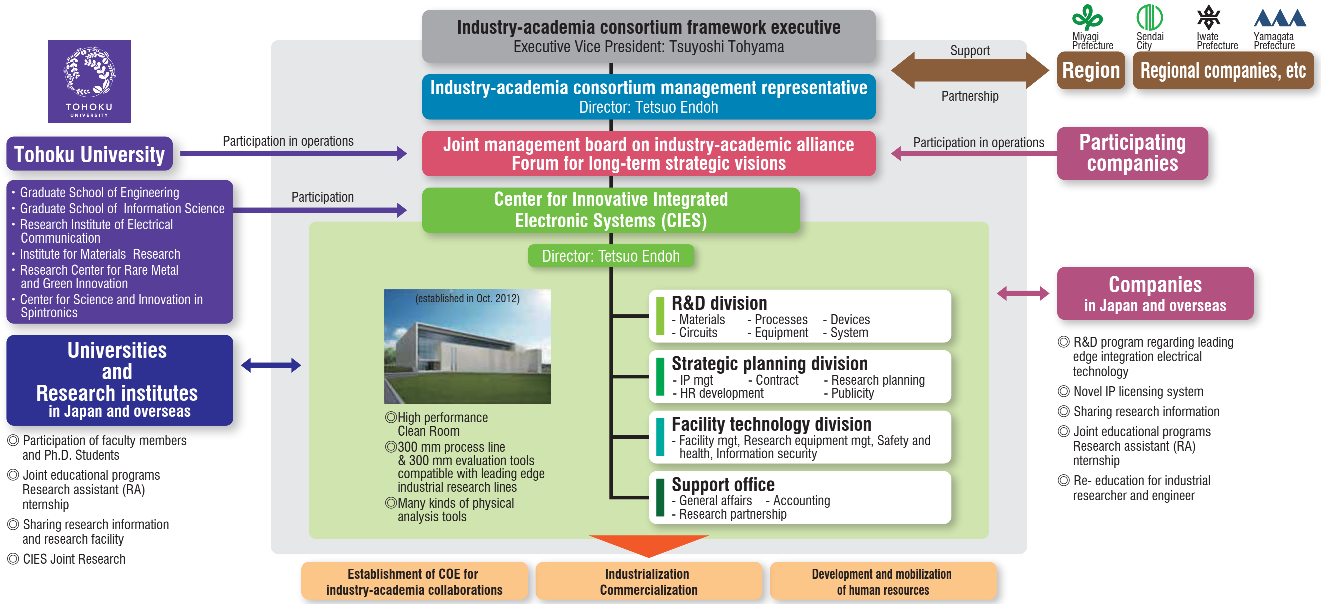
Green-based color: Ecology & low power

Meaning of "i": Innovation & integration

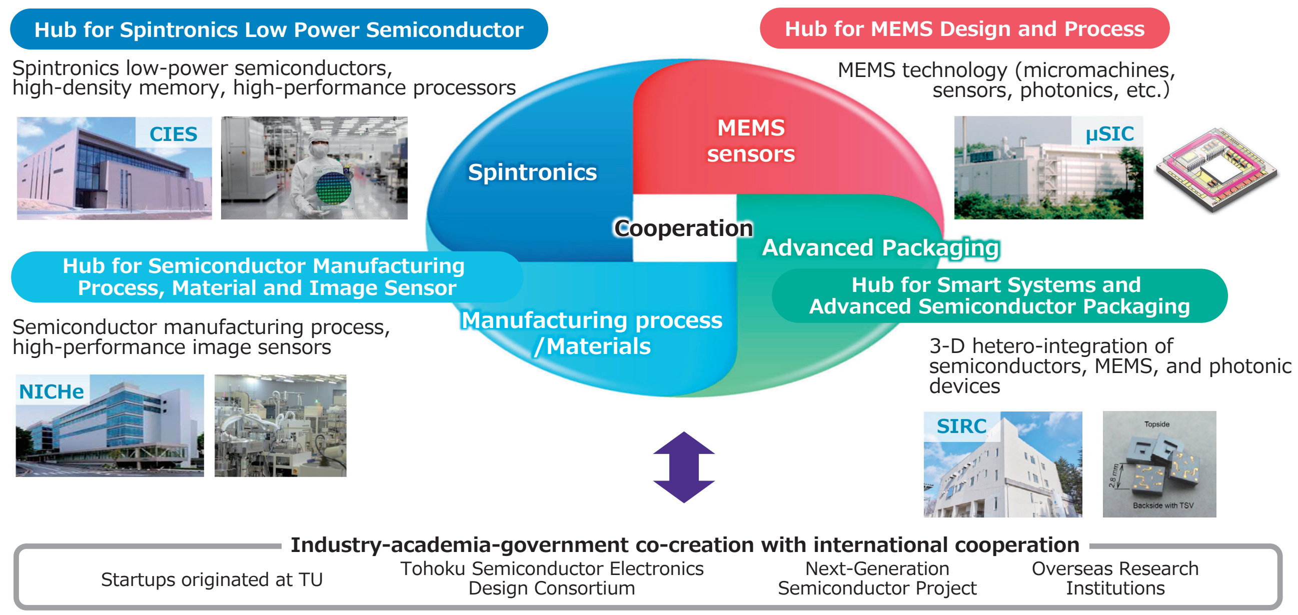
Three rings converging into " i ":

Integration of knowledge, science & technology with " i ",
Collaboration of industry, academia and government with " i ",
Combination of many kinds of layer researcher from material to system with " i "

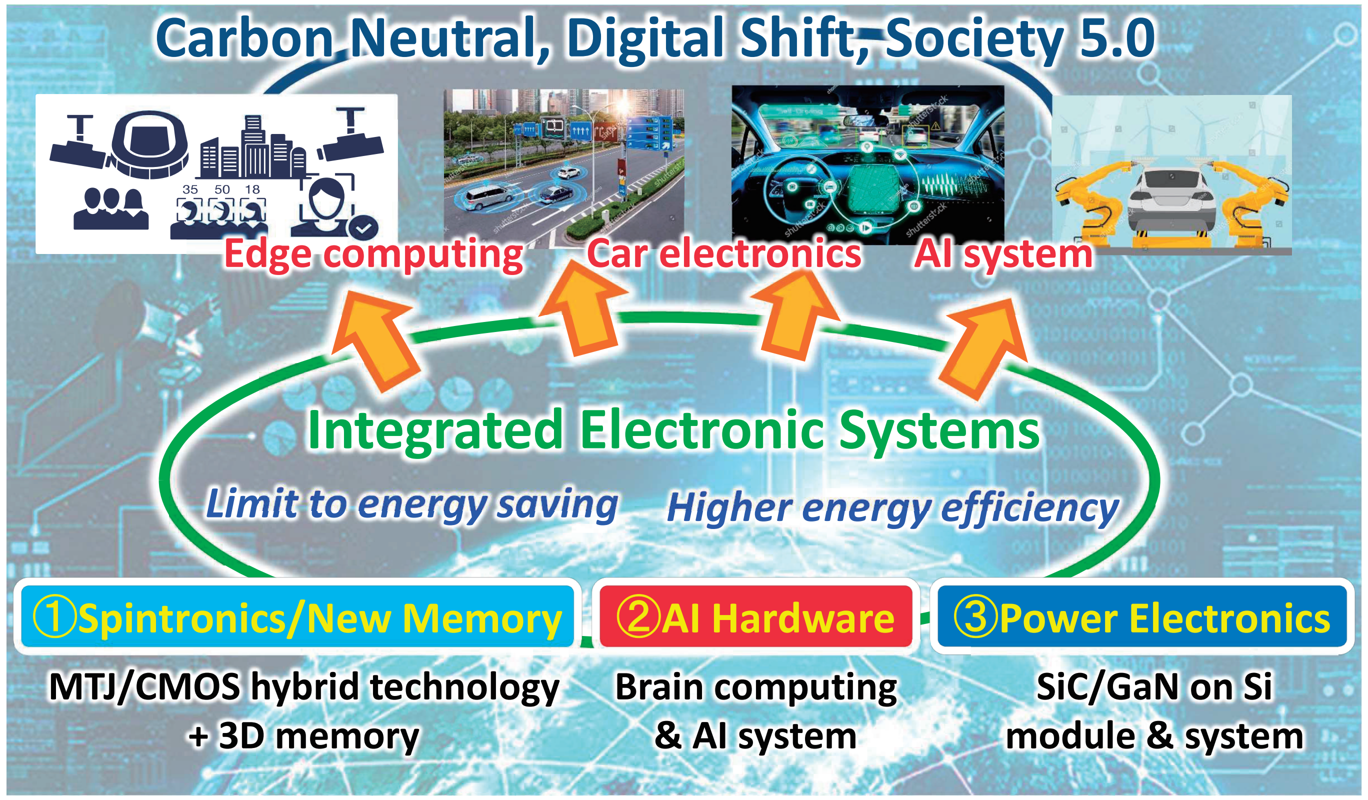
CIES Consortium



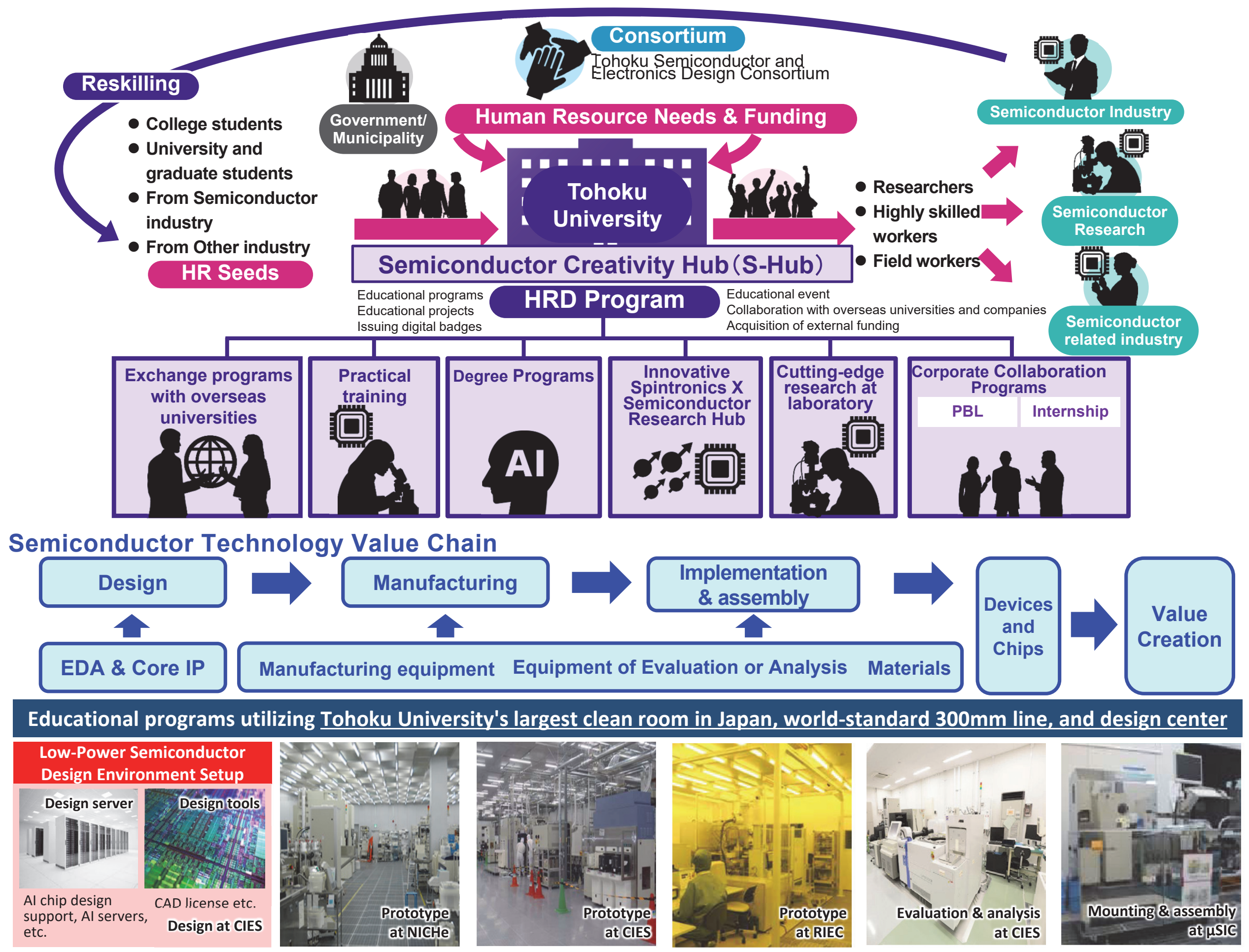
Tohoku Univ. Semiconductor Technology Co-creation



CIES R&D Scope



Tohoku Univ. Semiconductor Creativity Hub (S-Hub)



R&D Division (CIES Consortium)

A Industry-Academic Collaboration

Spintronics	LSI Technology	STT/SOT-MRAM & Spintronics/CMOS Hybrid processor	R&D of material and device technologies
			R&D of manufacturing technologies
			R&D of measurement, evaluation and analysis technologies
			R&D of circuit and design tool technologies
			R&D of STT-MRAM・SOT-MRAM and Spintronics/CMOS Hybrid application processor
		R&D of technologies to automatically design environments for low-energy consumption and highly functional VLSI processors based on non-volatile memory	
	Embedded Device Technology	R&D of supersensitive magnetic sensors using ferromagnetic tunnel junctions	
	System Technology	R&D of a VLSI platform for real-world intelligent integrated systems	
3D Memory	3D Integrated Circuit Technology	R&D of 3D non-volatile memory	
AI Hardware	Circuit Technology	R&D of brain-type processing circuit technologies	
		R&D of error correction technologies in flexible information processing	
		R&D of MTJ/CMOS Hybrid AI application processors	
Power Electronics	Device/ Module/ Circuit Technology	R&D of WBG power module technologies	
		R&D of next-generation electrical component technologies	
		R&D of integration and packaging technologies	

B National Projects

MEXT Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)	Innovative spintronics X semiconductor research hub
NEDO Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems	Development of advanced semiconductor manufacturing technology／Photonics-electronic convergence interface memory module technology
JAXA Space Exploration Innovation Hub	Standby power-free system by MTJ/CMOS Hybrid technologies and its environmental tolerance test (for space application)
JSPS Core-to-Core Program	Spintronics/Vertical elements of two-dimensional materials
MEXT Research and Development of Basic Technologies for Creating Innovative Power Electronics	Research and development of integrated power electronics for the realization of a decarbonized society
CAO SIP Project (3rd Phase)	Intelligent power electronics system with USPM to support grid stabilization

C J-Innovation HUB (International Development Category)

Center for Innovative Integrated Electronic Systems

D Community-based Cooperation Projects

Integrated Electronics Project	R&D of electronic device components for IT
Car Electronics Project	R&D of electronic device components for automotive
Tohoku Semiconductor Electronics Design Consortium	Human resource development and retention, resilience of supply chains

The Semiconductor Technology Co-creation Center	Co-creation Research Center	MEXT Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)

A Industry – Academic Collaboration　Spintronics　LSI Technology

R&D of STT/SOT-MRAM & Spintronics/CMOS Hybrid processor

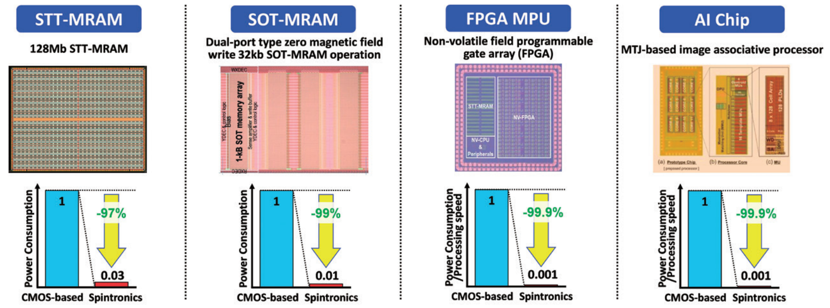

Prof. Tetsuo Endoh


Prof. Shoji Ikeda

In this R&D project, the technologies for STT/SOT-MRAM & Spintronics/CMOS Hybrid processor are researched and developed with combing the spintronics technology and the silicon CMOS technology, in joint efforts between industry and academia.

The actual R&D items are as follows. ①Material/device technologies for the spintronics devices that have a compatibility for CMOS integrated circuits, ②Unit process/process integration technologies using the industry-standard 300mm Si wafers, ③Highly efficient measurement/evaluation technologies and multifunctional analysis technologies, ④Circuit and design tool technologies that cover from basic memory cells to large scale integrated circuits.

By integrating these developed technologies, we have designed STT/SOT-MRAM, and microcontrollers and AI application processors such as image recognition processors using spintronics/CMOS hybrid technology, and have demonstrated low power consumption performance in their integrated circuits prototyped using 300mm process lines. From now on, we will continue to promote further technological innovation through this project. In this way, we will accelerate the practical application of nonvolatile working memory and nonvolatile logic, which will realize dramatic low-power systems, and contribute to the realization of a carbon neutral society.



A Industry – Academic Collaboration　Spintronics　LSI Technology

R&D of automated design environments for low-energy and highly functional VLSI processors based on nonvolatile storage


T. Hanyu prof

In order to overcome a power-wall problem in 4x-nm CMOS era and beyond, our R&D project aims to develop nonvolatile (NV)-device-based logic-circuit Intellectual Properties (IPs) and its automated design environment. The actual development items are as follows:

1. **Development of an automated-design CAD environment for NV-LSIs (cf. Figure right)**
   We are engaged in the development of an automated CAD environment for low-power and high-performance NV circuits and systems that integrate emerging back-end memory technologies such as MRAM.

2. **Development of a NV-based circuit IPs**
   We have also been developing logic-circuit IPs (LUTs, NV registers, etc.) for realizing a further energy-efficient/highly functional NV-LSI.

3. **Applications to AI accelerators**
   As an effective application, we are developing NV-based energy-efficient AI accelerators.

It is expected that the NV-LSI is utilized in a wide variety of applications such as IoT and mobile devices.

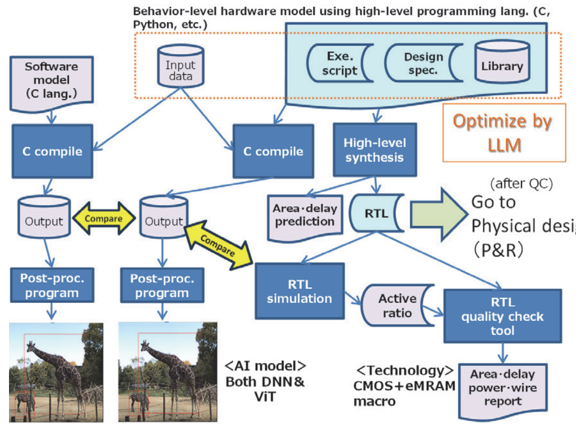
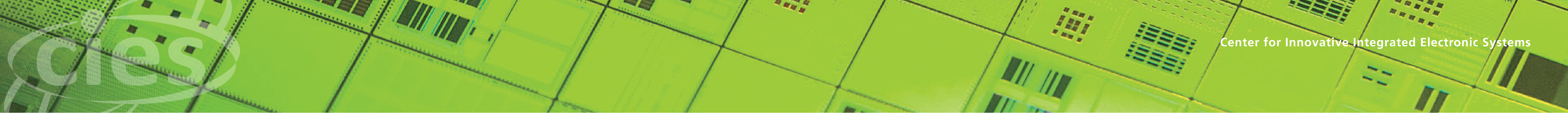


Figure: Example of an automatic circuit-design CAD environment based on high-level synthesis (C language). Utilizing C-language-based design assets, it is possible to design nonvolatile logic circuits/VLSI processors. As a result, it could become easy to explore the optimal design architecture for AI accelerators.



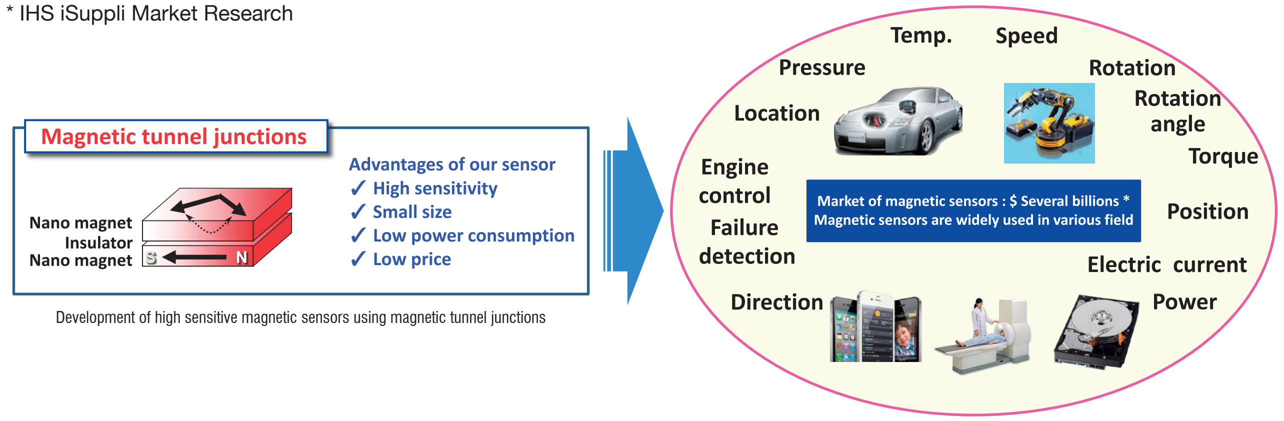
A Industry – Academic Collaboration Spintronics Embedded Device Technology

R&D of supersensitive magnetic sensors using ferromagnetic tunnel junctions


Prof. Yasuo Ando
Prof. Mikihiko Oogane

Magnetic sensors are widely used in various fields, such as environment, security, medical appliances, information technology, automobiles, etc. Additionally, the market scale of magnetic sensors is several billion dollars*. In this research, we will develop magnetic sensor devices with high sensitivity, small size, low power consumption and low cost using magnetic tunnel junctions (MTJs). A revolution in market of magnetic sensors is expected by realization of high-performance MTJs.

* IHS iSuppli Market Research



Development of high sensitive magnetic sensors using magnetic tunnel junctions

A Industry – Academic Collaboration AI Hardware Circuit Technology

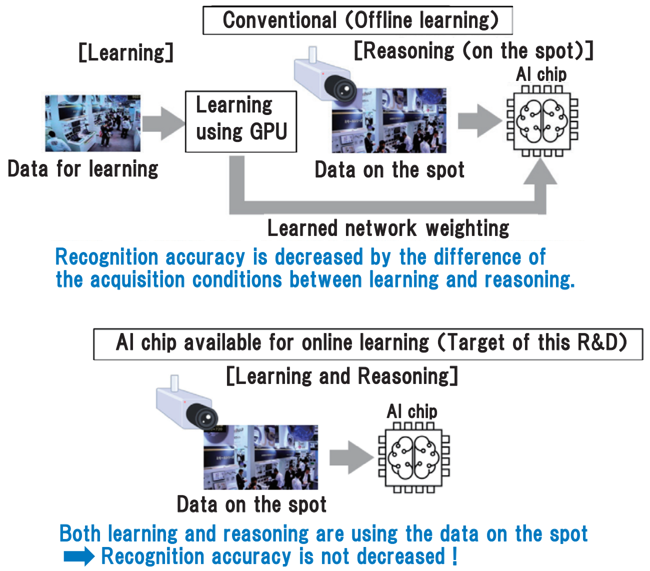
R&D of brain-type processing circuit technologies

Prof. Tetsuo Endoh

In this research and development, we have developed edge AI processors with low power consumption and high speed which are important for Society5.0.

In the conventional edge AI processors, after learning process which has been performed offline using GPU, learned parameter data have been used for inference process of AI chip. Generally, since the data acquisition conditions at inference (on the spot) are different with those at learning, the recognition accuracy of AI chip is always decreased.

In order to solve this problem, we have researched and developed the architecture / circuit / device technologies of the high-accuracy and ultra-high-speed edge AI processors which can learn and make an inference on the spot. MRAM attracts attention as nonvolatile memory, so we establish a base in the architectures / circuits to utilize MRAM thoroughly, and continue to develop the system-level fine-grain power gating, the high efficiency data transfer mechanism to dissolve data transfer bottleneck, the circuits / devices of MRAM suitable for uses, and the novel AI processor architectures with offline/online learning.

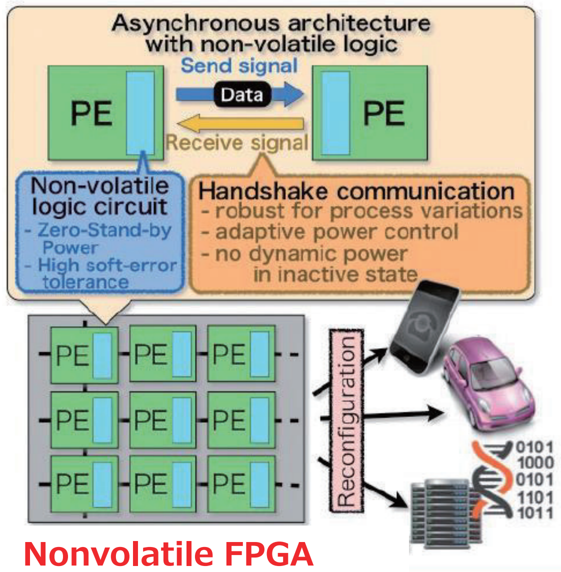


A Industry – Academic Collaboration Spintronics System Technology

R&D of a VLSI platform for real-world intelligent integrated systems

Prof. Tetsuo Endoh

The aim of our project is to develop a new reconfigurable LSI with low power, high performance and high soft-error tolerance for real-world intelligent systems, big-data applications and infrastructure applications. For state-of-art process technologies with smaller feature sizes, 3-D integration and an ultra low supply voltage, we develop synchronous/asynchronous hybrid circuits with autonomous supply-voltage control, MRAM-based non-volatile logic circuits for low stand-by leakage power and high soft-error tolerance, and high-level design tools that allow us to exploit easily reconfigurable LSI applications using these advanced circuit technologies.



Computer architecture by ultra-low-power reconfigurable LSI (FPGA) based on non-volatile logic with fine-grain power-control capability

A Industry – Academic Collaboration AI Hardware Circuit Technology

R&D of error correction technologies in flexible information processing

Prof. Tetsuo Endoh

In DRAMs and other storage devices, cosmic rays, temperature conditions, and other factors can cause the storage bits to flip, resulting in incorrect calculation results. ECC (Error Correction Code) technology has been developed to detect and correct these errors, by converting the original data into an error correction code with redundancy, which can detect errors and restore the original data. However, in order to increase the correction capability (i.e., to detect and correct more errors), a large amount of redundancy is required to match the capability (Fig. 1).

ECC technology is also used in "memory", an important component in computers, and in particular, memory that has an ECC circuit implemented as hardware is called ECC memory (Fig.2). Normally, the ECC algorithm called "SECDED", which is capable of correcting 1-bit errors and detecting 2-bit errors, has been commonly used in ECC memory. In this study, we have been exploring and verifying not only SECDED, but also the most suitable ECC algorithm with high correction capability for STT-MRAM based on software, which is easy to implement and improve by trial and error. The BCH code can select the number of bits that can be corrected under certain constraints. On the other hand, Golay codes can detect and correct errors and recover data with a simpler calculation than BCH codes, although the code length and the number of correctable bits are fixed.

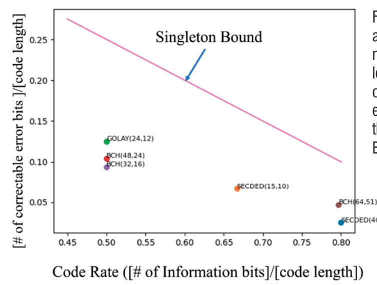


Fig.1 The horizontal and vertical axes are "code rate" and "the maximum number of correctable bits over code length", respectively. There is a trade-off relationship between the both. Any error-correcting code is never beyond the theoretical bound, called Singleton Bound.

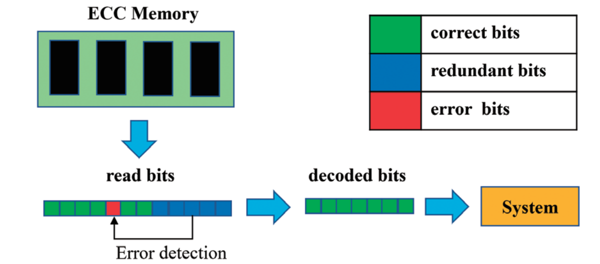


Fig. 2 A schematic figure of ECC Memory. The device can correct error bits in data and send the right data to the system, thanks to redundant bits included within the data.

A Industry – Academic Collaboration AI Hardware Circuit Technology

R&D of MTJ/CMOS Hybrid AI application processors

Prof.
Tetsuo Endoh

Advances in deep learning (DL) technology and parallel processors (e.g., GPUs) that can perform large-scale operations at high speed have made it possible to achieve highly accurate and fast object recognition, which was difficult until now (Figure 1). However, while these processors are capable of high-speed computation, they also consume a lot of power for accessing storage circuits, so it is necessary to reduce power consumption when installing them in in-vehicle computers and edge devices. Power consumption reduction can be expected by compressing and optimizing the DL algorithm. Furthermore, by applying power gating (PG), which takes advantage of the non-volatility of MTJ/CMOS hybrid circuits, power consumption reduction can be expected from power reduction during memory circuit access.

Therefore, we are developing a scheme to analyze the performance (recognition accuracy, speed, and memory access patterns) for DL algorithms running on various hardware (Figure 2). By analyzing memory patterns and improving algorithms suitable for PG, we aim to develop DL algorithms that match MTJ/CMOS hybrid circuit technology.

Fig.1 Object detection results recognized by one of famous algorithms, YOLOv3. The algorithm can detect small objects in the picture.

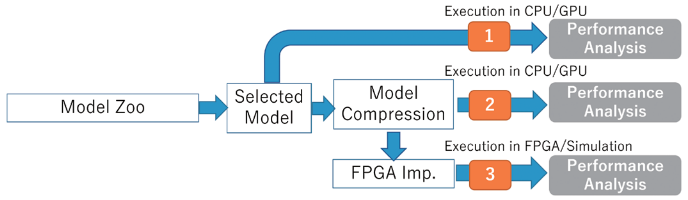


Fig. 2 A scheme of performance analysis of DL model selected from Model Zoo, being executed on CPU/GPU/FPGA. The analysis includes detection accuracy, speed and memory performance analysis, though which we try to select suitable DL models, and modify algorithm of those as well.

A Industry – Academic Collaboration Power Electronics Equipment Technology

Research and development of next-generation electrical equipment technology

Prof.
Yoshikazu Takahashi
Prof.
Tetsuo Endoh

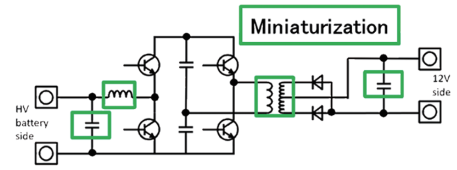
In this research theme, industry and academia are researching and developing DC-DC converters using GaN on Si lateral power devices that can be driven at high frequencies.

This contributes to the realization of a highly efficient and ultra-compact DC-DC converter that can handle the increased power supply due to the increase in the number of sensors and actuators associated with the progress of automated driving in automobiles.

We are developing the following technologies.

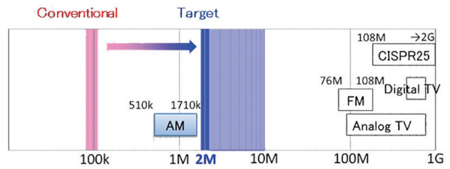
1. High-frequency drive technology for DC-DC converters
   Development of high-frequency drive technology using ultra-high-speed GaN on Si lateral power devices that enables downsizing of passive components such as passive components such as isolation transformers, reactors, and capacitors in DC-DC converter.
2. Low noise technology
   Reduction of noise filter (miniaturization of DC-DC converter) by driving DC-DC converter at high frequency (2MHz or higher) above AM radio frequency band, and development of optimum driving technology to suppress ringing noise.
3. High power technology
   Development of parallel connection operation technology and multiphase operation technology for GaN on Si devices

Miniaturization of passive device by high frequency



DCDC converter circuit

Reduction of AM radio noise filter by 2MHz drive



DCDC converter operating frequency for commercial frequency band

A Industry – Academic Collaboration Power Electronics Module Technology

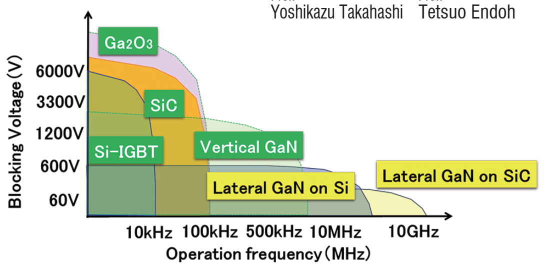
Research and Development of WBG Power Module Technology

Prof.
Yoshikazu Takahashi
Prof.
Tetsuo Endoh

In this research theme, industry-academia collaboration is underway to develop power module technology that maximizes the features of wide bandgap (WBG) power devices such as SiC-MOSFETs and GaN on Si lateral power devices, which combine low loss and high speed. This will contribute to the realization of high-performance electric vehicles (EVs), compact and high-efficiency power supplies for data centers, and smart cities that optimize power supply operations.

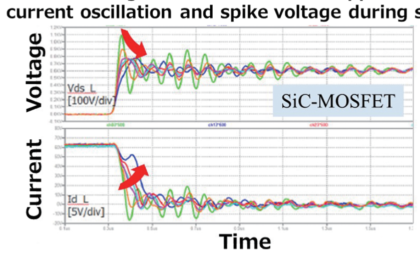
Following technologies are being developed.

1. Voltage and current oscillation suppression technology for WBG power modules
   Development of low-inductance module technology to suppress voltage and current oscillation and spike voltage during switching while taking advantage of the high-speed performance of WBG power devices.
   Development of active gate drive circuit technology.
2. low thermal resistance technology
   Development of high thermal conductivity insulating substrate technology to suppress temperature rise during high frequency operation of WBG power chips, which are becoming smaller and higher power density.
3. high heat dissipation technology
   Development of new air-cooled and water-cooled cooler technologies to cope with the increasing capacity of WBG power devices.



Relationship between operating frequency and breakdown voltage of various power devices (conceptual diagram)

Optimized active gate control function suppresses voltage and current oscillation and spike voltage during switching



A Industry – Academic Collaboration Power Electronics integration Technology

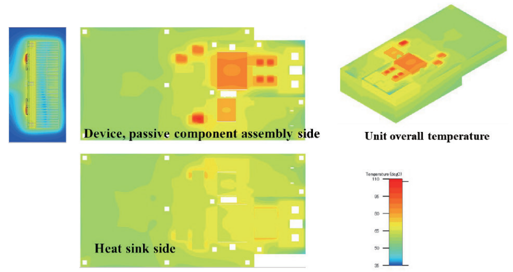
R & D on assembly integration technology

Prof.
Yoshikazu Takahashi
Prof.
Tetsuo Endoh

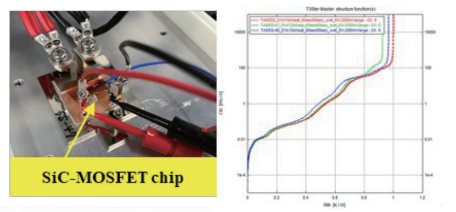
In this research theme, industry and academia collaborate on research and development of assembly integration technologies to take advantage of the superior characteristics of new WBG devices such as GaN-on-Si and SiC. This contributes to reducing the size, weight, functionality, and performance of power electronics equipment.

We are developing the following technologies.

1. Passive component technology
   Development of low loss / ultra-small reactor and transformer technology with low iron loss and copper loss even when driving at high frequencies, and development of capacitor technology that can withstand high temperatures of 250 degrees or higher.
2. Power integrity technology and high heat dissipation layout technology
   Development of power integrity technology for various PCB substrates applied to high integration density power electronics circuits.
   Development of high heat dissipation layout technology that does not increase chip temperature at high frequency
3. Bonding materials and technology
   Development of low thermal resistance and high reliability bonding materials and technology for assembling GaN on Si devices, gate circuits, and various passive components on insulating substrates and cooling structures.



High heat dissipation layout technology



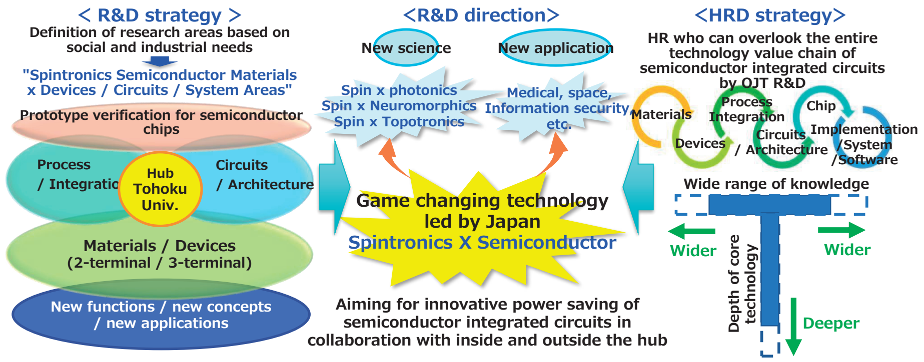
Evaluation of transient thermal resistance of different bonding materials

B National Project MEXT Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)

Innovative spintronics X semiconductor research hub

Prof.
Tetsuo Endoh

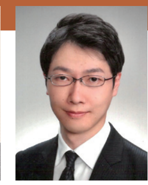
We will put spintronics, which is a game change technology for low-power integrated circuits led by Japan, at the core. We will comprehensively conduct from R&D of new materials and devices, R&D of circuits, architectures and integrated technologies that bring out their characteristics, to prototype verification for low-power semiconductor chips that accelerate the development of CMOS semiconductors with collaborative and cooperating organizations. While promoting this activity, we will lead the creation of new science and the transformation of the information society by cultivating the fusion area of electronics with light / neuro / topology, and pioneering new applications such as medical care, space, and information security, and then contribute to the improvement of our research and development capabilities related to semiconductors. We have young researchers and students actively and strategically participate in this hub, and develop human resources who have the practical ability and a bird's-eye view.



Overview of the hub concept

B National Project JAXA Space Exploration Innovation Hub

Standby power-free system by MTJ/CMOS hybrid technologies and its environmental tolerance test (for space application)



Prof.
Tetsuo Endoh

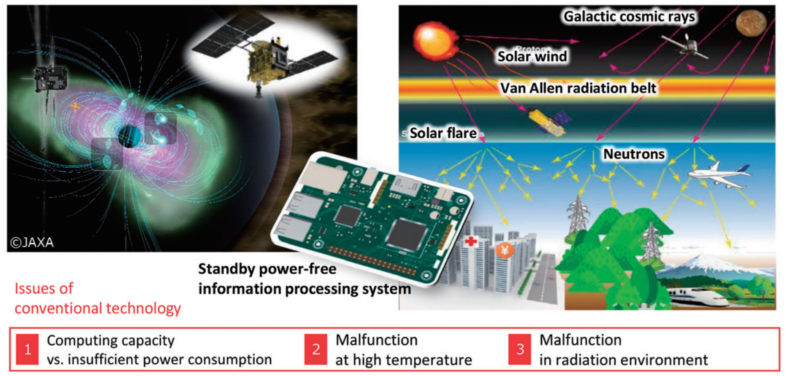
Associate Prof. (JAXA)
Daisuke Kobayashi

A research proposal "Standby-power-free system by MTJ/CMOS hybrid technology and its environmental resistance test (for space applications)" by CIES, Tohoku University in FY2019 was selected for the request for proposal (RFP) by the JAXA Space Exploration Innovation Hub to expand "the human sphere of life and active area by exploring the solar system frontier". The project was selected as a follow-up research in FY2021, and is accelerating research and development.

For space exploration beyond Moon and Mars, long-term missions of more than 10 years are expected in environments where solar energy is weak, so ultra-low power electronic systems that cannot be achieved with existing technologies is required. Another important issue for spacecraft electronic systems is the need for both standby power and space radiation resistance.

In this proposal, we will research a system that does not require standby power using MTJ/CMOS hybrid technology that integrates CMOS technology and MTJ, which is a spintronic device developed by us. We aim to realize innovative semiconductor devices and integrated circuits that improve efficiency and reduce power consumption by orders of magnitude. Specifically, we will conducted the research on the materials for higher performance and higher reliability, and the MTJ/CMOS hybrid devices/circuits/integration process/chip technologies.

Based on the reliability evaluation including radiation tolerance test by JAXA, we aim to create a power-free integrated circuit that has environmental tolerance in addition to the non-volatility and high speed in MTJ/CMOS hybrid chips. This contributes to the solution of the research theme "Research on Standby Powerless Systems" specified by JAXA.



Research on standby power-free information processing system with radiation tolerance using MTJ/CMOS hybrid technology

B National Project NEDO Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems

Development of advanced semiconductor manufacturing technology

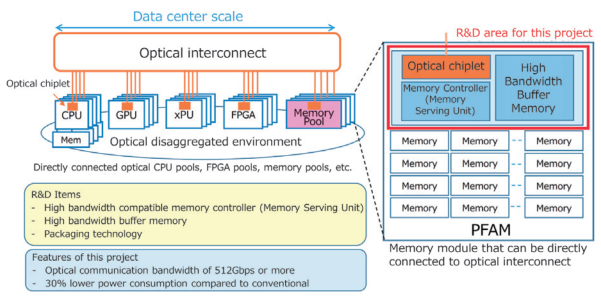
Photonics-electronic convergence interface memory module technology

Prof.
Tetsuo Endoh

Tohoku University will participate in a project as a subcontractor after the "Photonics-electronic convergence interface memory module technology" jointly proposed by Kioxia Corporation and NTT was adopted in NEDO Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems.

In the IOWN initiative promoted by NTT, data centers require disaggregated computing, which connects multiple computing resources (such as CPUs and GPUs) directly to optical interconnects in order to efficiently process a wide variety of real-time requests from multiple users. Additionally, memory must be shared by multiple computing resources to improve usage efficiency.

In this technology development, Tohoku University has subcontracted part of the technology development of photonic fabric attached memory module (PFAM), which realizes memory that can be accessed by broadband optical access from multiple computing resources via optical interconnect.



B National Project Core to core project

Research Center Formation Project – A. Advanced Center Formation Type -

"Spintronics/Vertical elements of two-dimensional materials"

Prof.
Tetsuo Endoh

This research theme proposes new vertical devices by integrating current spintronics technology with two-dimensional materials in order to create the next generation of spintronics technology. The aim is to integrate distinctive research of Japan, the UK, France and the US. Tohoku University plays a central role in collaborating with universities in Japan, France, the United Kingdom, and the United States.

1. UK-Japan collaboration

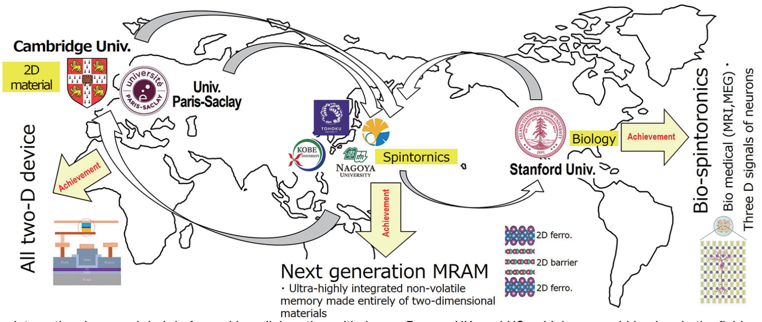
The University of Cambridge in the UK has world-class film formation technology and theoretical analysis of two-dimensional materials. By combining this with Japanese spintronics technology, we create vertical junction devices with a new two-dimensional material.

2. France-Japan collaboration

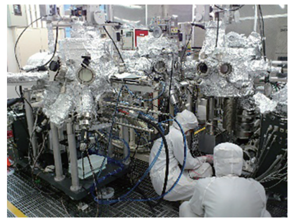
Albert Fert Institute and the University of Paris-Saclay in France have been conducting cutting-edge fundamental research and theories on spintronics, led by Dr. Albert Felt, who won the Nobel Prize in Physics in 2007. In this research, new spintronics devices are created by using advanced cutting-edge processing technology for two-dimensional materials.

3. Japan-US cooperation

Japanese group collaborated with Stanford University, the School of Engineering, and the School of Medicine, on new applications of spintronics devices, such as detecting firing signals leaking from neurons.

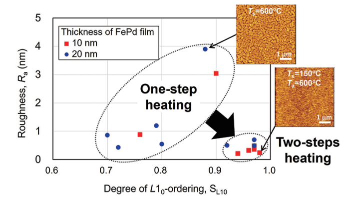


An international research hub is formed in collaboration with Japan, France, UK, and US, which are world leaders in the fields of spintronics, two-dimensional materials, and biology.

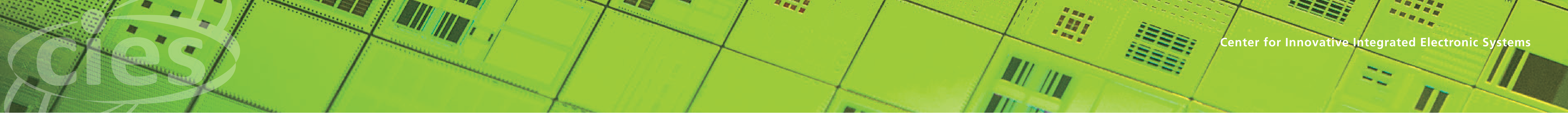


Equipment for depositing ordered alloys as spintronic layers

High-quality spintronics thin films successfully fabricated by two-step heating method.

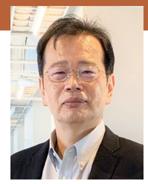


S. Vergara, H. Naganuma, J. Crys. Growth, (2025) *in-press*



B National Project | MEXT Research and Development of Basic Technologies for Creating Innovative Power Electronics

Research and development of integrated power electronics for the realization of a decarbonized society



Prof.
Yoshikazu Takahashi

This research theme aims to research and develop circuit systems that take full advantage of the superior performance of WBG devices to the limit, and to realize smaller size, higher performance, higher power density, and higher efficiency in next-generation inverters and power supplies through the development of ultra-compact, high-performance power modules, power unit and the application of optimal passive components.

Applied products include motor drive inverters for EVs, small and medium-sized inverters for industrial use, and power supplies for data centers, which are widely used in society to handle small and medium power ranges.

Tohoku University, which is the representative institution, Ibaraki University and Waseda University, which are research-sharing institutions, and an advisory board as a cooperating company will promote research and development on five sub-themes that are important for power electronics research.

By advancing these research and development efforts, we will create next-generation power electronics technologies and products that will lead the world and contribute to the realization of a decarbonized society.

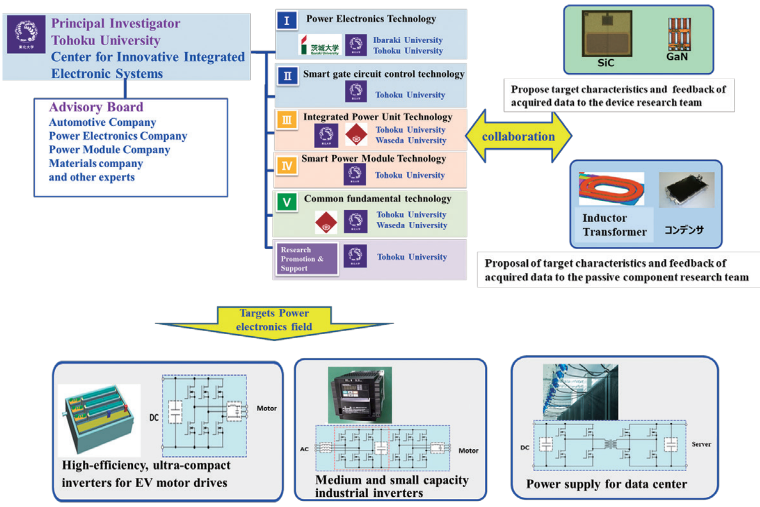


Fig.1 R&D system for integrated power electronics to realize a decarbonized society.

C J-Innovation HUB (International Development Category)

Activities for J-Innovation HUB initiative (International development category)

J-Innovation HUB

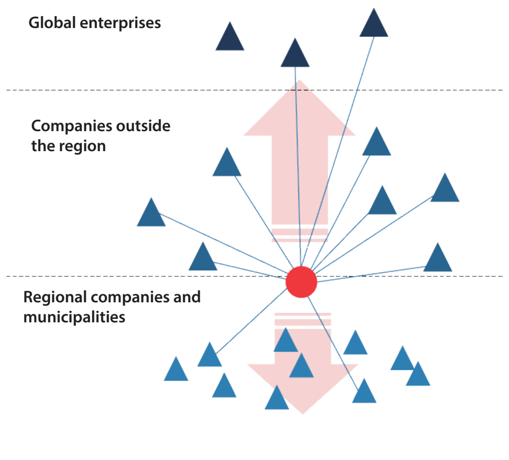
Prof.
Tetsuo Endoh

CIES was selected as the 1st industry-academia base of the "J-Innovation HUB Initiative", a project of the Ministry of Economy, Trade and Industry (METI) launched in 2020 (International development category).

Under this initiative, METI targets regional innovation hubs (mainly universities), and assesses and selects outstanding industry academia bases that are playing a leading role as hubs for networks of companies. The aim is to enhance their creditworthiness, focus public support measures on them, and enhance the capabilities of the top ranking hubs. METI selects the hubs in two categories: the international development category and the regional contribution category.

METI will advance dialogues with each of the selected hubs and will provide them with tailor-made support measures, including budgets and relaxation of regulations.

Partners participating in the activities of CIES are expected to take advantage of the preferential treatment of this J-Innovation HUB policy.



International development category Hub

(Source: Ministry of Economy, Trade and Industry)

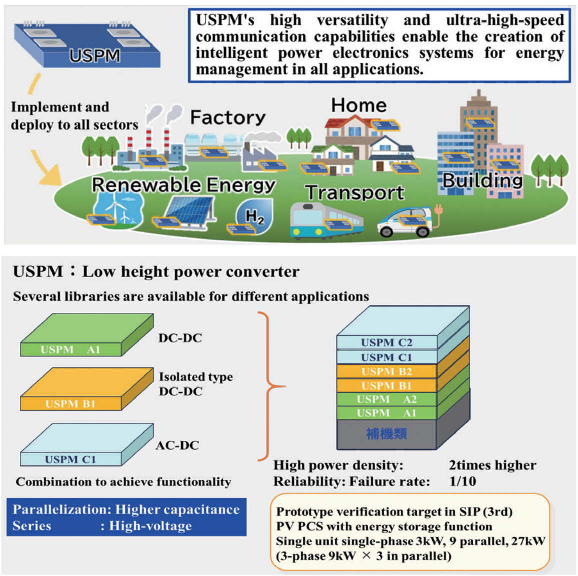
B National Project | Cabinet Office Cross-ministerial Strategic Innovation Promotion Program (SIP) 3rd

Intelligent power electronics system with USPM to support grid stabilization

Prof.
Yoshikazu Takahashi

Prof.
Shuji Katoh

This R&D aims to develop elemental technologies for next-generation high power density USPMs with a wide range of energy management (EMS) applications and grid stabilization functions, as well as application technologies for smart inverters and smart power supplies. Nagaoka University of Technology is the lead organization for this research and development, and Tohoku University CIES is in charge of developing reliability-enhancing technologies for next-generation USPMs through optimal packaging technology as a joint research institute. Specifically, we are working to suppress jump voltage and reduce noise during switching by reducing the inductance of power device packages applied to next-generation USPMs, and to achieve high integration with gate circuits and passive components in pursuit of a compact and easy-to-handle structure. In addition, in order for the next-generation USPM to contribute to the stabilization of the power system, it is necessary to respond to synchronization and pseudo-inertia forces as a grid-forming inverter. We will conduct research and development on package structures and gate drive methods that enable suppression of heat generation and temperature rise and overvoltage suppression of power semiconductor chips during high-current operation, which are essential for improving the synchronization and pseudo-inertia of next-generation USPMs. By advancing these R&D activities, we will contribute to the construction of intelligent power electronics systems with USPMs that support grid stabilization.



D Community-based Cooperation Project | Integrated Electronics | Car Electronics

Promotion of regional cooperation in integrated electronics and car electronics fields

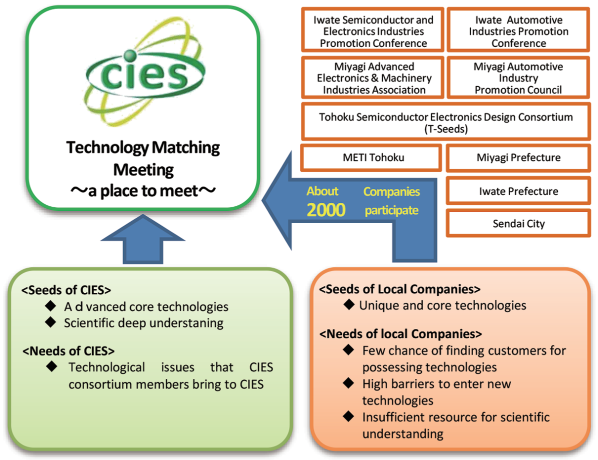
Prof.
Tetsuo Endoh

This activity aims to spread excellent core technologies of local companies to the world with cooperation of local government and administrative agencies. In particular, the following activities have been promoted.

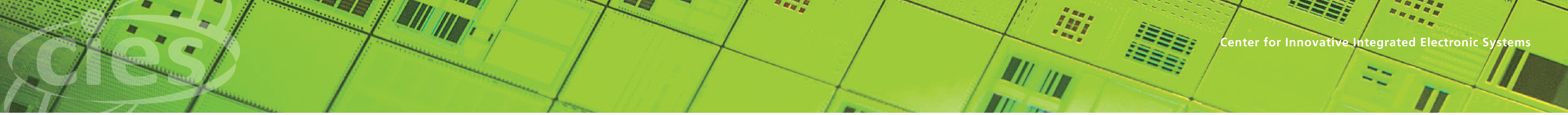
1) Sophisticate core technologies of local companies by integrating fundamental technologies and scientific knowledge of CIES;
2) Develop cooperation among local companies in electronics and automotive field, and apply the core technologies to new application, and work on study meeting of commercialization in cooperation with Miyagi and Iwate Prefectural Government ;
3) Promote cooperation between local companies and world-class companies at CIES as a place to meet, and spread the core technologies of local companies to the world.

Under these activities, unique core technologies by local companies will be applied to integrated electronics and car electronics, and the application and commercialization of the innovative devices will be promoted to next generation of IT and car electronics.

CIES will continue to contribute to Tohoku promotion.



Basic policy of the Community-based cooperation

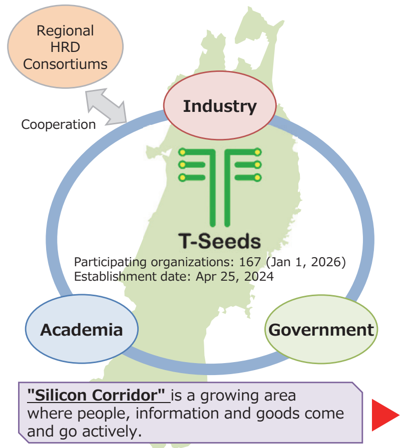


D Community-based Cooperation Project | Tohoku Semiconductor Electronics Design Consortium

Contribution to the Tohoku Semiconductor Electronics Design Consortium (T-Seeds)

Prof.
Tetsuo Endoh
T-Seeds Advisor

The Tohoku Semiconductor Electronics Design Consortium (T-Seeds) was formed as an industry-academia-government collaboration to strengthen the foundations of semiconductor-related industries in the Tohoku region and Japan. T-Seeds will work to create a "Silicon Corridor" where people, information, and goods flow actively and where regions and industries can grow synergistically. T-Seeds will promote efforts to expand the base of human resources in the semiconductor-related industry and to strengthen and develop the infrastructure, aiming to maximize the economic ripple effects.



"Silicon Corridor" is a growing area where people, information and goods come and go actively.

Expanding the base of human resources
- Curriculum tailored to students' interests and levels of proficiency
- Raising awareness among young people
- Early education for high-level personnel such as semiconductor designers

Strengthening and developing the infrastructure
- Measures to maintain performance of semiconductor manufacturing equipment
- Needs matching (e.g. equipment x parts, etc.)
- Considering measures for logistics, CN, etc.

✓ Growth of the region and semiconductor-related industries
✓ Maximizing economic ripple effects
【An important area for semiconductors thatwill support the future of Japan and the world】

Source: Tohoku Bureau of Economy, Trade and Industry

Co-creation Research Center

Co-creation Research Centers in the field of power electronics

Fuji Electric x Tohoku Univ. Advanced Technology Co-creation Research Center
Tohoku University and Fuji Electric Co., Ltd. established the Fuji Electric x Tohoku Univ. Advanced Technology Co-creation Research Center in November 2024 to promote research activities in the fields of power electronics and power semiconductors aimed at realizing a decarbonized society. In addition to conducting research on high-efficiency, compact power modules as well as power supply and drive systems, the institute will explore joint research themes focused on creating new value that contributes to the realization of a decarbonized society.

Specially Appointed Prof.
Tatsumi Kawata

Prof.
Yoshikazu Takahashi

Prof.
Tetsuo Endoh

Sumitomo Bakelite x Tohoku Univ. Co-creation Research Center for Materials and Processes for Next-Generation Semiconductors
Tohoku University and Sumitomo Bakelite Co., Ltd. established the Sumitomo Bakelite x Tohoku Univ.Co-creation Research Center for Materials and Processes for Next-Generation Semiconductors in January 2025. Through end-to-end research activities encompassing materials and material design, processes, performance evaluation, and social implementation for power modules, power devices, and AI-related devices, the institute aims to create new value and contribute to societal advancement.

Specially Appointed Prof.
Toshiharu Kuboyama

Prof.
Yoshikazu Takahashi

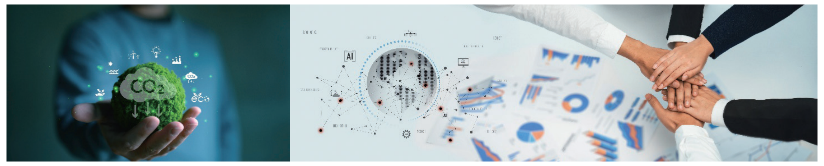
Prof.
Tetsuo Endoh

Tamura x Tohoku Univ. Advanced Power Electronics Co-creation Research Center
Tohoku University and Tamura Corporation established the Tamura x Tohoku Univ. Advanced Power Electronics Co-creation Research Center in October 2025 with the aim of promoting research and development of materials, components, devices, and modules that create new value in the power electronics market. Through joint research and development, the partners are working to create new magnetic passive components differentiated at the materials level, enabling high-efficiency, high-power, and high-frequency operation compatible with wide-bandgap (WBG) semiconductors.

Specially Appointed Prof.
Tatsuya Kiyota

Prof.
Yoshikazu Takahashi

Prof.
Tetsuo Endoh



The Semiconductor Technology Co-creation Center

Toward Japan's largest semiconductor R&D ecosystem

Prof.
Tetsuo Endoh

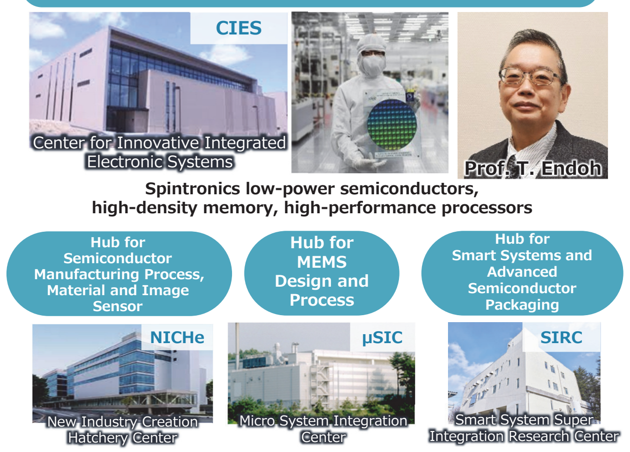
○ Background and purpose
In order to contribute to strengthening the international competitiveness of Japan's semiconductor industry, the Tohoku University Semiconductor Technology Co-Create center will leverage its openness as a university to share the university's diverse results with various institutions, creating synergies and building an R&D ecosystem.

○ Initiative details and effects
This co-creation organization has four hubs, and our Center for Innovative Integrated Electronic Systems is one of them, as a "Hub for Spintronics Low Power Semiconductor". We are responsible for the design, prototype demonstration, and evaluation of low-power logic semiconductors and AI processors, high-density memory, and high-performance processors, as well as its system development. In addition, Tohoku University has the "Hub for Semiconductor Manufacturing Process, Material and Image Sensor" based on ultra-clean process technology and image sensor technology, the "Hub for MEMS Design and Process," which is responsible for R&D, technical evaluation, and prototyping of various devices and advanced mounting technology, and the "Hub for Smart Systems and Advanced Semiconductor Packaging. We collaborates with these three centers to lead semiconductor research in Japan.
https://semicon.tohoku.ac.jp/en/

Semiconductor Technology Co-creation
Tohoku Univ.'s Overwhelming Strengths

- Top level semiconductor research, Group of ca. 150 researchers
- Unmatched R&D resources, e.g. large clean rooms(8,500m²)

Hub for Spintronics Low Power Semiconductor



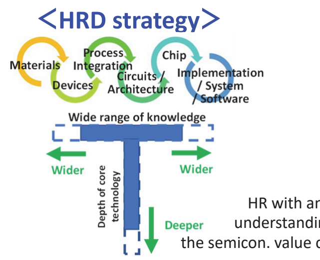
MEXT Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)

Semiconductor Human Resource Development
at Innovative Spintronics X Semiconductor Research Hub

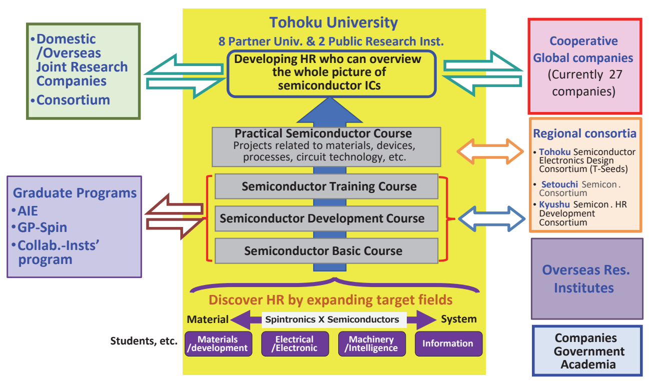
Prof.
Tetsuo Endoh

Prof.
Toshiro Kaneko

Background: Part of MEXT's X-NICS project, this initiative addresses the global shortage of talent in energy-efficient semiconductors through industry-academia-government collaboration.
Objective: It aims to cultivate highly skilled human resources with comprehensive knowledge of spintronics-based semiconductors, covering materials, devices, circuits, and evaluation, along with business awareness required by industry.
Content: The program features multi-level courses, internships, and industry-led OJT. We have also established the X-nics HRD Support Fund to provide financial aid for doctoral students.
Expected Impact: By boosting researchers' practical skills and industry networks, the program accelerates the social implementation of new technologies and strengthens Japan's semiconductor competitiveness.

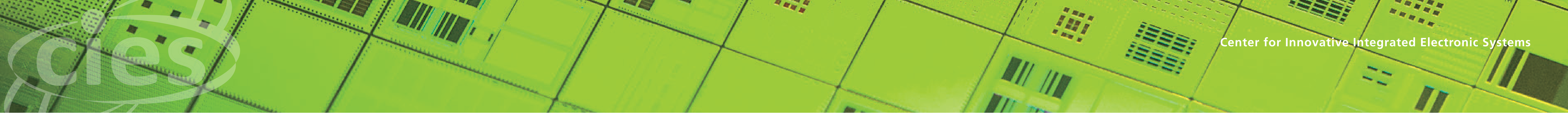


An open badge will be issued to students who complete all four courses.



Course Outline Examples : Outstanding Leader Seminar I

	Lecture title
1	R&D of Medical Devices and Medical Information Solutions
2	Data-Driven R&D -Business Management and Technology Development-
3	DX Initiatives in companies
4	GenAI and Its Corporate Strategies
5	GenAI vs. SIer - The Current State and Potential of On-Site Use
6	Utilizing AI Technology in Broadcasting
7	Challenging the Revolution in Steelmaking: Case Studies of AI & Data Science
8	Text Mining - Research and Application of AI & GenAI to Businesses
9	R&D at Companies in the Fire and Disaster Prevention Field
10	HMI Product Development and the Use of AI Technology
11	Traffic Flow Sensing and Data Analysis Using LiDAR Technology
12	Contributions of DX and Electronics to Infrastructure Businesses
13	OSS Models and Utilizing GenAI



Advanced Human Resource Development Program

The following programs have been implemented with the objective of developing young research resources in the field of integrated electronics technology.

① Lectures and curriculum delivered by industry-academia joint faculties (credit courses)

In these courses, we explain the types of talents required in industry sectors and society as a whole, create curriculum based on those principles, and offer lectures by members of industry-academia joint faculties.

② Participating in Tohoku Semiconductor Electronics Design Consortium

We participate in Tohoku Semiconductor Electronics Design Consortium responsible for the human resource development etc. in Tohoku established by Ministry of Economy, Trade and Industry.

③ Industry-academia collaboration OJT system promoting advanced human resource development

●RA system within the CIES consortium

We elucidate the responsibilities of people engaged in industry-academia collaborative research and aim to encourage graduate sudents /postdoctoral / young researchers to participate in industry-academia collaborative research by providing compensation.

X-nics RA Students

●RA System within X-nics

Human resources with business sense and an overview of the entire technological value chain of semiconductor integrated circuits, including materials, devices, design, circuits, architecture, integration technology, prototyping, evaluation, and systemization, who can also deepen their own understanding of core technologies and specialized fields.

●Internship system

A promotion system has been organized targeting doctoral course students (DCs), post-doctoral fellows (PDs), and young faculties etc., to help to take part in internships at companies participating in CIES consortium.

④ Participating in University program

●Center for Science and Innovation in Spintronics (CSIS)

In the certification of "Designated National University", the CSIS is aiming to establish a hub that pioneers new field of "Spin-Centered Science" in the world by strategically gathering outstanding researchers through international collaborations.

●Center for Spintronics Research Network, Tohoku University (CSRN)

The CSRN is aiming at the formation of research network hub to promote collaborative research with domestic and international institutes for accelerating international competitiveness of world-leading spintronics research, creating new industries, strengthening the current industry and developing next generation human resources.

●Graduate Program in Spintronics, Tohoku University (GP-Spin)

This program aims to foster researchers who can play an active role internationally in spintronics area which is our strength research field. This program is supervised by world leading professors including CIES members.

●Tohoku Forum for Creativity

We participate in a university program that develop human resources who can start a business or play an active role in a company through the research. The program cultivates not only fundamental business skills like management and communication but also advanced skills like setting issues and solving problems.

Facility Technology Division

Facility technology division focuses on four main functions in order to achieve safety, stable, and efficient research and development. Not only gas and liquid leakage, particle sensor management, in/out security control for research zone, but also 24 hours monitoring of electricity, gas and water can provide safe and validity research and development circumstance.

We operate a clean room with a 300mm wafer process line. Management duties include daily inspections to ensure stable and safe operations. Maintenance is carried out to ensure stable operation of the 300mm wafer process equipment installed in the clean room.

As for ensuring safety, safety education is conducted to the facility and equipment users. To provide instruction and improve safety and health, we established a safety and health committee, safety patrols, and evacuation drills.

As for information security, we manage network security for information equipment in CIES and also provide education to facility and equipment users.

Facility Technology Division

- **Facility management** — 300mm process line / Supply facilities
- **Research quipment management** — 300mm process equipment / 300mm evaluation tools
- **Safety and health** — Safety and health committee / Safety patrols / Evacuation drills
- **Information security** — Information control / Information leak control / Information security literacy

Strategic Planning Division

Strategic planning division establishes flexible joint research frame work in order to operate it efficiently and actively, based on the world-class core technologies and experienced administration support.

Intellectual Property (IP), which are core IP and emerging new IP, can be managed as our valuable asset and enable to provide them for consortium members efficiently. Based on this new IP system, flexible and global standard joint research contracts are ready for domestic and overseas companies.

Strategic Planning Division

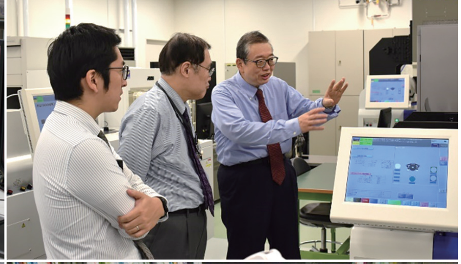
- **Practical IP management** — IP pool / share / acquired sub-systems
- **Contract** — Flexible and global standard
- **Research planning** — Attractive and sustainable topics
- **HR development** — Internship with cooperated companies
- **Publicity** — Public relations for networking

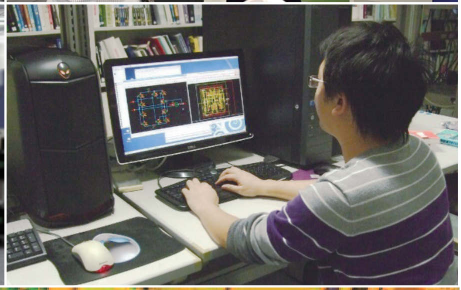
Tohoku University Center for Innovative Integrated Electronic Systems

Spintronics Low-Power Semiconductor Design Center in Aobayama Universe

Power Electronics Division, Center for Innovative Integrated Electronic Systems, Tohoku University (located within Research Center for Rare Metal and Green Innovation, Tohoku University)





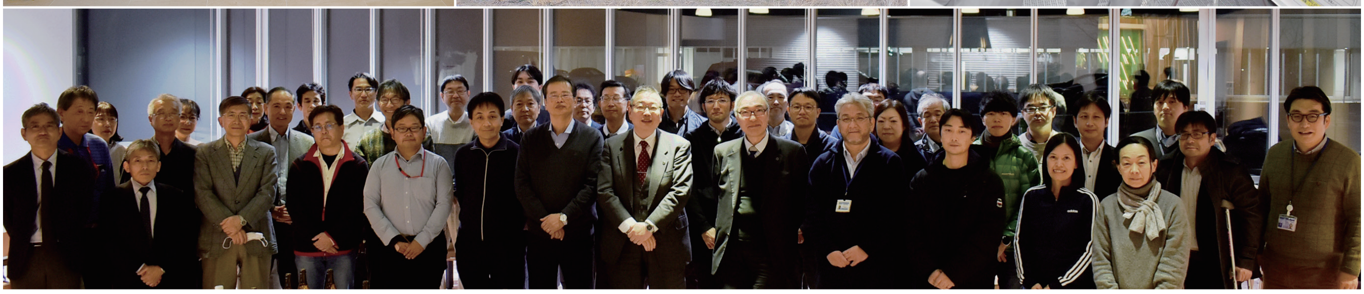



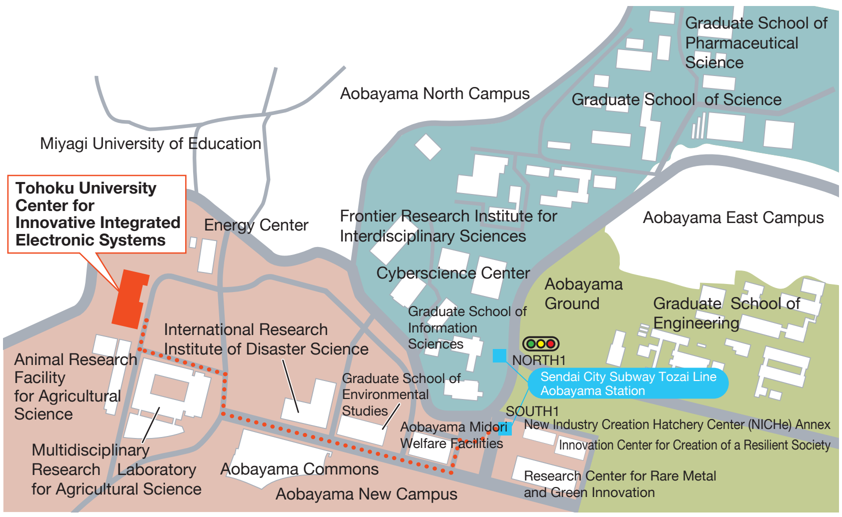
The center of excellence (COE) of academic-industrial alliance networking the world-wide intelligence and creating new knowledge of humankind by innovative integrated electronics and sophisticated-training-based education











Access

By Subway
Please take subway Tozai Line bound for “Yagiyama Zoological Park Station” from “Sendai Station”, and get off subway at “Aobayama Station”. (about 9 mins ride) Please go out from Exit South 1, and it is about 10 minutes’ walk from “Aobayama Station” to CIES.

Contact

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Center for Innovative Integrated Electronic Systems

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