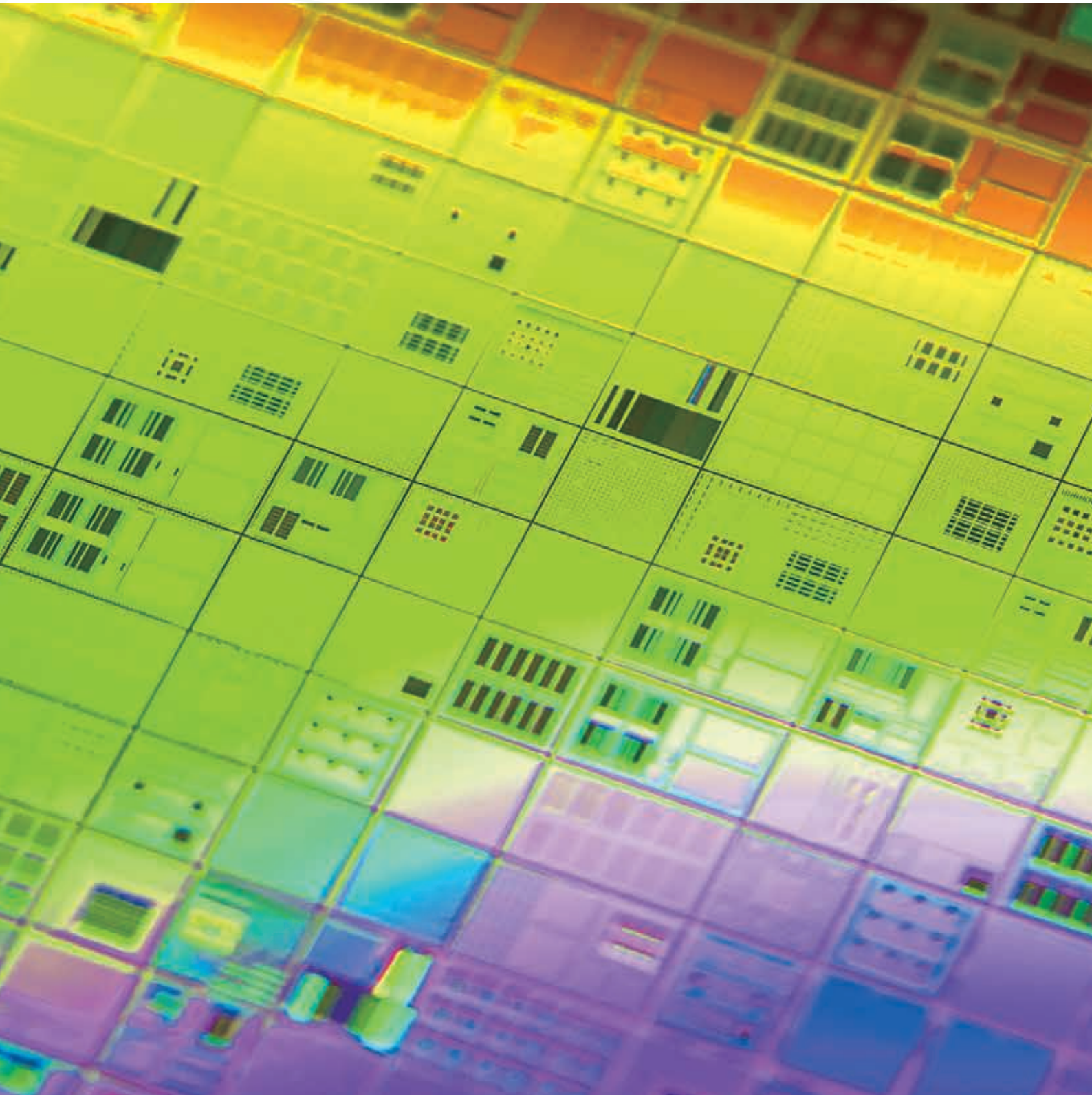
2020-2022 EDITION

東北大学 国際集積エレクトロニクス研究開発センター

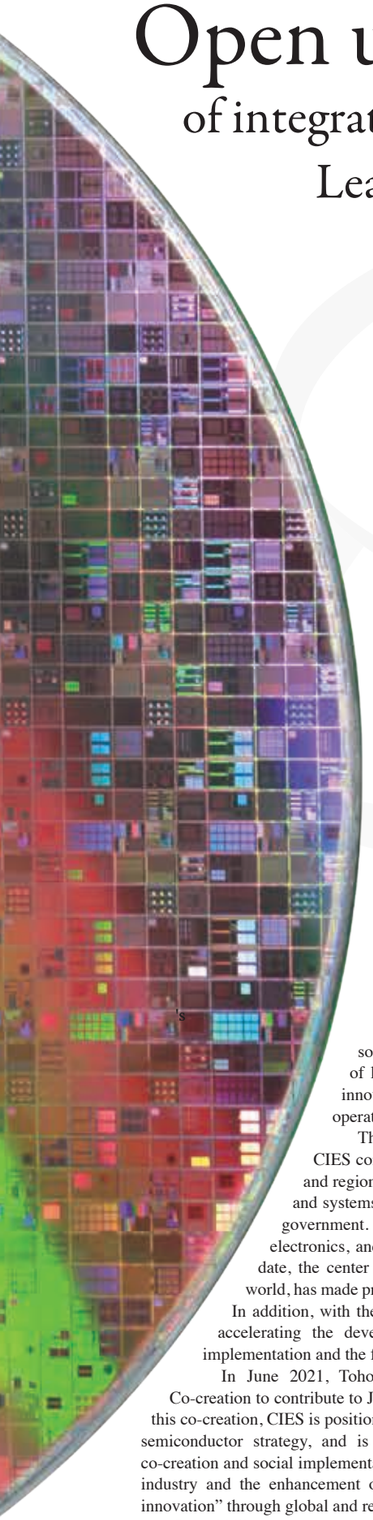
Tohoku University Center for Innovative Integrated Electronic Systems



Open up Innovation

of integrated electronics from the international industry-a cademic alliance!

Lead the recovery and new creation　　Leap towar d world-class



feature
Hardware

First privately donated research and development center by founded Tohoku University in Science Park

300mm wafer process line, facilities for device, characterization & physical analysis in university campus for the first time in Japan

*1 Official support from Miyagi Prefecture through the system of special zones for the promotion of private investment (information service related industries) that was applied for jointly by the Miyagi prefectural government and municipal governments in the prefecture.

*2 Official support from Sendai City through an amount corresponding to the fixed property tax, etc., according to an agreement made by Tohoku University and Sendai City.

Our Mission and Vision

The Center aims to contribute to the enhancement of global competitiveness in the field of next-generation integrated electronics systems, and work toward the creation of practical applications and new industries, through the research and development of innovative devices and its integrated electronic systems and constructing a consortium for this field under the international collaboration among industries, universities and government.

fe ature
Sof tware

Flexible joint research frame work between industry-academic alliance

Knowledge based on accomplishments between academic-industrial collaborations

Centralized administrative control and strategic operation of world-class intellectual properties of core technologies

Global standard joint research contracts

feature
Core technology

Advanced core technolo gies and intellectual properties from materials/devices/ p rocesses to system/architectures, created and reserve d at Tohoku University under its "Research First" prin ciple and "Open Doors" philosop hy, and "Practice-Oriented Research and Education" ethos.

- Materials technology
- Device technology
- Fabrication technology
- Circuit design technology
- System design technolo gy
- Software technology
- Algorithm technology

etc.

The integrated electronic systems are exploited for every industrial products and social infrastructure, and are the fundamental technology which determine the quality of life. To meet social needs such as carbon neutrality, AI/IoT/DX, and Society 5.0, innovative integrated electronics systems that can achieve dramatic power-saving operations are required.

The Center for Innovative Integrated Electronic Systems (CIES) has conducted the CIES consortium consisting of industry-academia joint researches, major national projects, and regional collaboration projects from fields such as materials, equipment, devices, circuits and systems through the cooperation of domestic and foreign companies with support of local government. CIES has expanded its R&D field from spintronics to AI hardware and power electronics, and has promoted to develop core technologies related to integrated electronics. To date, the center has developed various innovative technologies with highest performance in the world, has made progress in developing IoT and AI systems that require ultra-low power consumption. In addition, with the establishment of the startup "Power Spin Inc." from Tohoku University, we are accelerating the development of the innovative technologies that we are developing into social implementation and the further advancement of industry-academia collaboration.

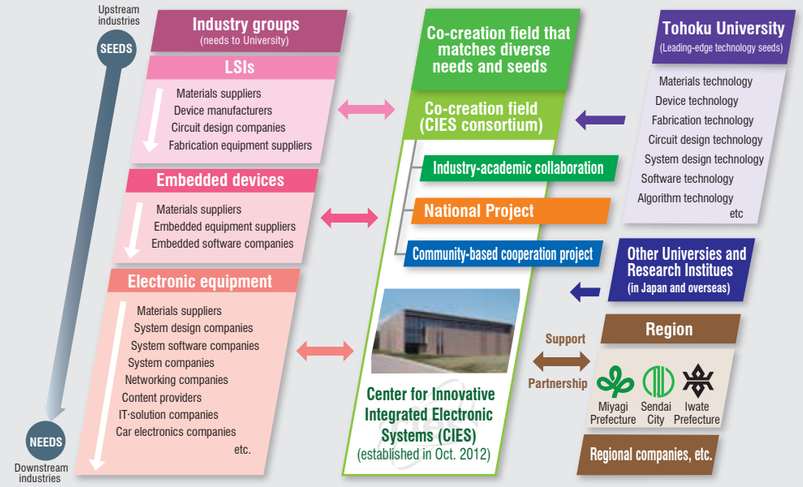
In June 2021, Tohoku University established the Tohoku University Semiconductor Technology Co-creation to contribute to Japan's semiconductor strategy and the world's energy-saving society. In addition to this co-creation, CIES is positioned as a spintronics power-saving logic semiconductor development base in Japan's semiconductor strategy, and is further strengthening efforts for promotion of industry-academia-government co-creation and social implementation. We will continue to create innovative core technologies and contribute to the industry and the enhancement of global competitiveness by the practical applications, and "new creation and innovation" through global and regional partnership.

I would like to express my deepest gratitude to all for your dedication and continued support.

March 2022

Tetsuo Endoh
Director of CIES

Goal of the center : Model "B-U-B (Business-University-Business)"



In order to create innovative integrated electronics technology and power electronics technology that respond to energy conservation society and support the upcoming Big Data, IoT, Artificial Intelligence (AI) era, it is necessary to continuously create new growth principles and to promote industry-academia collaboration that combines scientific understanding (ability of science) and advanced manufacturing ability (productivity). It is essential to upgrade and expand the places.

In view of this social requirement, this center builds an international industry-academia collaborating base around the world with a wide range of research seeds accumulated by the university and abundant industry-academia cooperation achievements as a centripetal force, a co-creation field (CIES consortium). We will promote R & D of innovative technologies that will contribute to the future energy-saving society, safety-safe society, etc. Among these, industry-academia cooperation collaborations with various world class domestic and foreign enterprises from upstream industries (materials / processes / ULSI etc.) to downstream industries (software / equipment / systems etc.). In collaboration with large national projects responsible for R & D in the field, local public entities (Miyagi prefecture, Sendai city, Iwate prefecture, etc.), we will develop regional collaboration projects with regional and local companies and support measures from national and regional administration. We also continue to create new core technology groups, contributing to practical application and industrialization of innovative seed technology. Through these efforts, we will create a synergistic effect through collaboration among researchers in a wide range of fields and create a technology supply chain of hierarchical needs and seeds in the future.

CIES symbol and its messages

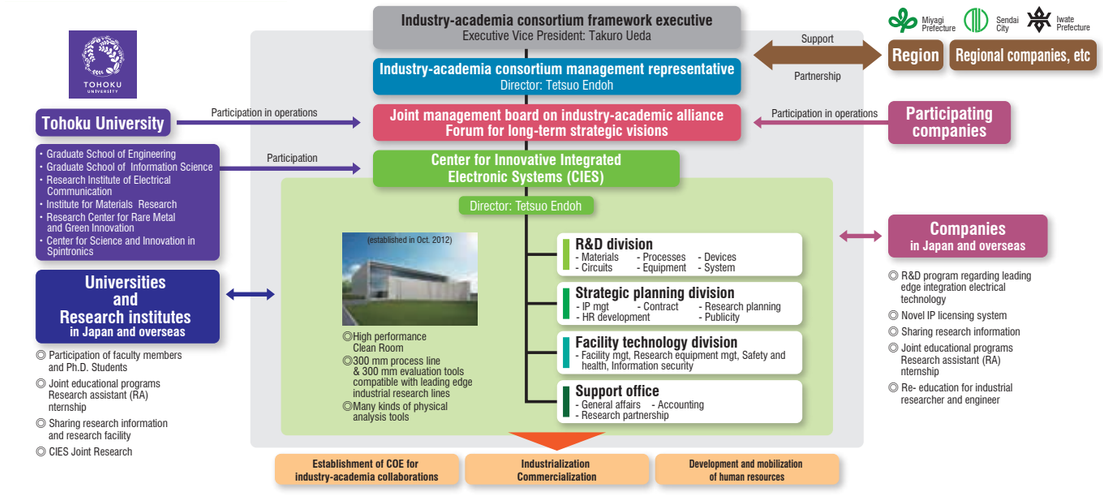
cies
Center for Innovative Integrated Electronic Systems

Symbolic messages

Green-based color: Ecology & low power
Meaning of "i": Innovation & integration
Three rings converging into " i ":
Integration of knowledge, science & technology with " i ",
Collaboration of industry, academia and government with " i ",
Combination of many kinds of layer researcher from material to system with " i "

CIES Consortium R&D Scope

Organization of CIES Consortium



Ultra-low power spintronics logic semiconductor development hub

Consistent development from design, prototyping, evaluation, and system Creation of world-leading power-saving technology through development and demonstration

Leading the world in the development of spintronics logic semiconductors and their application systems

The world's only 300mm compatible R & D facility in semiconductor development spintronics logic

Power consumption of logic semiconductors reduced to 1/100

Design innovation | Collaboration with TIA / Fundry | Innovation in materials and manufacturing technology | Innovation in evaluation technology | System innovation

Spintronics logic design → CMOS manufacturing → Spintronics material / device manufacturing → Spintronics logic evaluation demonstration → System development utilizing advanced spintronics logic

Bringing further innovation

Contribution to strengthening industrial competitiveness through social implementation

【 Venture from Tohoku University 】

Cooperation

Semiconductor manufacturing process / dmaterial / image sensor development demonstration hub

MEMS design / process development demonstration hub

Tohoku univ. modell

A virtuous cycle of funds by creating new Industries through innovative technology from Tohoku Univ. and accelerating social implementation

Innovative technology from Tohoku Univ. Spintronics semiconductors

- Creating markets for spintronics semiconductor manufacturing / evaluation equipments and design tools
- Creation of low-power chip design market by circuit IP and architecture of spintronics semiconductors

Technology recipient:
- From domestic and overseas semiconductor-related industries to semiconductor user companies
- Tohoku University startup "Power Spin Inc."

Core technology: Spintronics + CMOS
Tohoku univ. New AI / IoT spintronics semiconductor prototype line

- Creating a power-saving semiconductor / system market that contributes to carbon neutrality

R&D Division (CIES Consortium)

A Industry-Academic Collaboration

Spintronics	LSI Technology	STT/SOT-MRAM & spin device/CMOS Hybrid processor: R&D of material and device technologies
		R&D of manufacturing technologies
		R&D of measurement, evaluation and analysis technologies
		R&D of circuit and design tool technologies
		R&D of STT-MRAM・SOT-MRAM and MTJ/CMOS Hybrid application processor
		R&D of technologies to automatically design environments for low-energy consumption and highly functional VLSI processors based on non-volatile memory
	Embedded Device Technology	R&D of supersensitive magnetic sensors using ferromagnetic tunnel junctions
		R&D of ultra-small full-spin 3-D wireless semiconductor embedded substrate (SESUB) technologies featuring power saving
	System Technology	Basic research on image processing technology for next-generation automobiles and information appliances
		Research and development on embedded security technology
		R&D of a VLSI platform for real-world intelligent integrated systems
3D Memory	3D Integrated Circuit Technology	R&D of 3D non-volatile memory
AI Hardware	Circuit Technology	R&D of brain-type processing circuit technologies
		R&D of error correction technologies in flexible information processing
		R&D of MTJ/CMOS Hybrid AI application processors
Power Electronics	Device/ Module/ Circuit Technology	R&D of GaN on Si power device technologies
		R&D of GaN on Si power module technologies
		R&D of next-generation electrical component technologies
		R&D of integration and packaging technologies
		R&D of next-generation high-power converters for power and industry

B National Projects

MEXT Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)	Innovative spintronics X semiconductor research hub
NEDO Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems	Feasibility study / Research and development of microfabrication core technologies for nonvolatile MRAM at 1.5nm node and beyond
NEDO Leading Research for Discovering R&D Issues	AI chips/next-generation computing that enables high efficiency and high speed processing / Computing technology using CMOS/spintronics Hybrid technology
NEDO Strategic Innovation Program for Energy Conservation Technologies	Practical application development / Development of high-speed non-contact AI thermal camera for multi-personnel detection for post COVID-19 hazardous map creation
Tohoku Bureau of Economy, Trade and Industry Strategic Basic Technology Advancement Support Program	Development of spintronics/CMOS Hybrid LSI design technology and software, and their productization
JAXA Space Exploration Innovation Hub	Standby power-free system by MTJ/CMOS Hybrid technologies and its environmental tolerance test (for space application)
CAO SIP Project (2nd Phase)	"Physical space digital processing platform" R&D of ultra low power IoT devices and its technical platform with MTJ/CMOS Hybrid technologies for Society 5.0
JST OPERA Project	World-leading open innovation platform of fusion technologies bridged IT and transportation system areas
JSPS Core-to-Core Program	Controlled interfacing of 2D materials for integrated device technology
MEXT Research and Development of Basic Technologies for Creating Innovative Power Electronics	Research and development of integrated power electronics for the realization of a decarbonized society

C J-Innovation HUB

International development category／Center for Innovative Integrated Electronic Systems

D Community-based Cooperation Projects

Integrated Electronics Project	R&D of electronic device components for IT
Car Electronics Project	R&D of electronic device components for automotive

A Industry – Academic Collaboration Spintronics LSI Technology

R&D of STT/SOT-MRAM & spin device/CMOS Hybrid processor

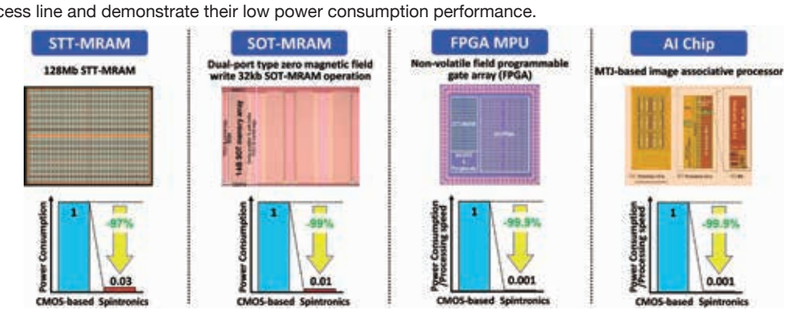

Prof. Tetsuo Endoh


Prof. Shoji Ikeda

In this R&D project, the technologies for STT/SOT-MRAM & spin device/CMOS Hybrid processor are researched and developed with combing the spintronics technology and the silicon CMOS technology, in joint efforts between industry and academia. The aim of the project is to accelerate the realization of nonvolatile working memory and nonvolatile logic that will make super low power electronic systems possible and to contribute to the realization of carbon neutral society.

The actual R&D items are as follows. ①Material/device technologies for the spintronics devices that have a compatibility for CMOS integrated circuits, ②Unit process/process integration technologies using the industry-standard 300mm Si wafers, ③Highly efficient measurement/evaluation technologies and multifunctional analysis technologies, ④Circuit and design tool technologies that cover from basic memory cells to large scale integrated circuits.

We integrate the above technologies and design AI application processors, for instance, micro computers and image recognition processors using STT-MRAM/SOT-MRAM and spin device/CMOS hybrid technologies. In addition, we manufacture them experimentally by 300mm process line and demonstrate their low power consumption performance.



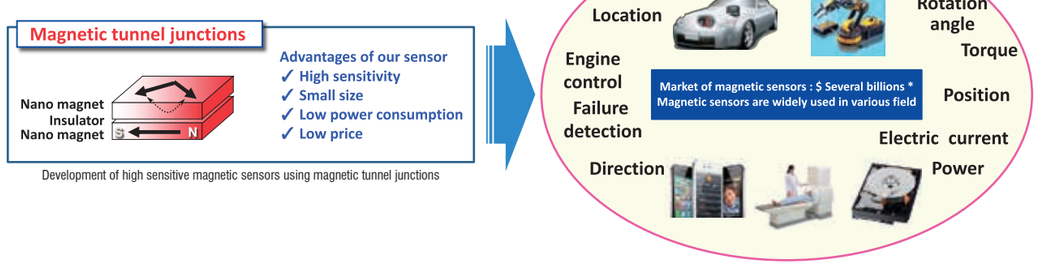
A Industry – Academic Collaboration Spintronics Embedded Device Technology

R&D of supersensitive magnetic sensors using ferromagnetic tunnel junctions


Prof. Yasuo Ando

Magnetic sensors are widely used in various fields, such as environment, security, medical appliances, information technology, automobiles, etc. Additionally, the market scale of magnetic sensors is several billion dollars*. In this research, we will develop magnetic sensor devices with high sensitivity, small size, low power consumption and low cost using magnetic tunnel junctions (MTJs). A revolution in market of magnetic sensors is expected by realization of high-performance MTJs.

* IHS iSuppli Market Research



Development of high sensitive magnetic sensors using magnetic tunnel junctions

A Industry – Academic Collaboration Spintronics LSI Technology

R&D of technologies to automatically design environments for low-energy consumption and highly functional VLSI processors based on non-volatile memory


Prof. Takahiro Hanyu


Associate Prof. Daisuke Suzuki

To overcome a power-wall problem in 4x-nm CMOS era and beyond, our R&D project aims to develop nonvolatile (NV)-device-based logic-circuit Intellectual Properties (IPs) and its automatic design environment. The actual development items are as follows:

1. Development of a CAD environment for NV-FPGAs

FPGAs (Field-Programmable Gate Array) is a attractive hardware platform for various applications. We have been establishing the environment by combining an open-source CAD tool, called Verilog-to-Routing (VTR), with nonvolatile logic-circuit IPs.

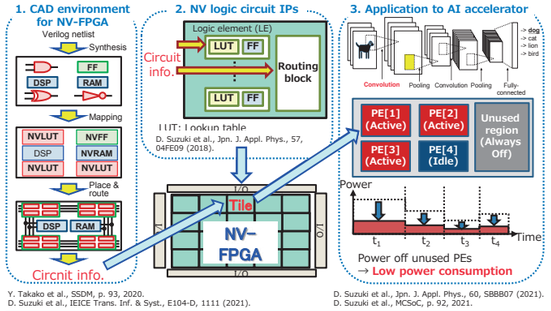
2. Development of a NV-based circuit IPs

We have also been developing logic circuit IPs for realizing a further energy-efficient/highly functional NV-FPGA.

3. Applications to AI accelerators

As an effective application, we have been developing NV-FPGA-based energy-efficient AI accelerator.

It is expected that the NV-FPGA is utilized in a wide variety of applications such as IoT and mobile devices.



Y. Takako et al., SSDM, p. 93, 2020.
D. Suzuki et al., IEICE Trans. Inf. & Syst., E104-D, 1111 (2021).

D. Suzuki et al., Jpn. J. Appl. Phys., 60, SBBB07 (2021).
D. Suzuki et al., MCSoC, p. 92, 2021.

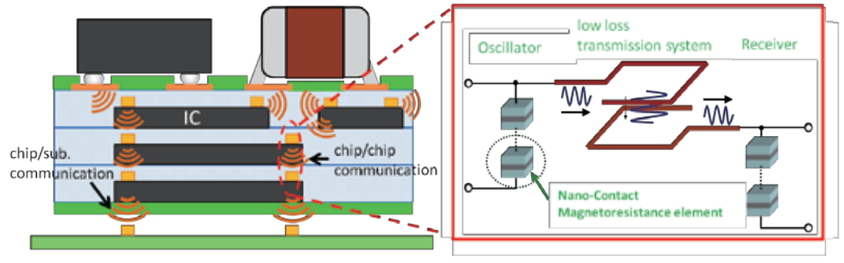
1. CAD environment for effectively implementing user defined hardware
2. Improvement of NV-logic circuit IP for higher energy efficiency and functionality
3. Application to AI accelerators and NV-FPGA oriented energy-efficiency improvement

A Industry – Academic Collaboration Spintronics Embedded Device Technology

R&D of ultra-small full-spin 3-D wireless semiconductor embedded substrate (SESUB) technologies featuring power saving


Assistant Prof. Yohei Shiokawa

In 3D integration among IC chips with heterogeneous function, there is an urgent need for wireless communication because of downsizing, power saving, and low cost. In this research, we will develop the spin-torque oscillator / receiver by using Nano-Contact Magnetoresistance device and transmission technology between oscillator and receiver for 3D-IC integration technology as wireless SESUB (Silicon Embedded Substrate) technology. The issues of this research development are to create the higher power / higher sensitivity spin-torque oscillator / receiver and to construct the low loss transmission system with electromagnetic resonance antenna. After solving these problems, we will actualize the full-spin wireless SESUB.



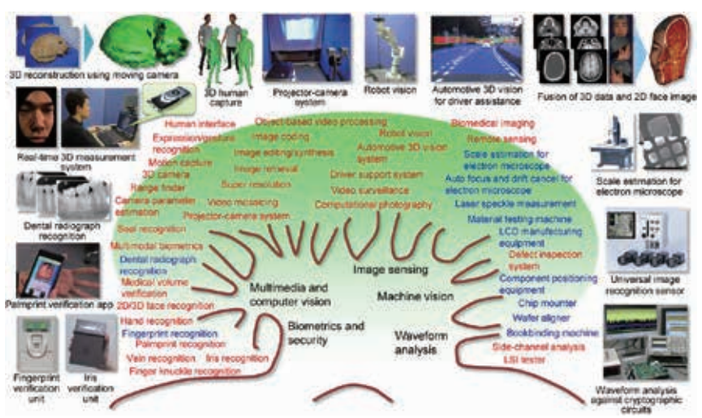
Schematic illustration of full-spin 3D wireless SESUB(Semiconductor embedded in SUBstrate)

A Industry – Academic Collaboration Spintronics System Technology

Basic research on image processing technology for next-generation automobiles and information appliances

Prof.
Takafumi Aoki

This R&D project aims to study the fundamental technologies of 2D/3D-fused visual information processing for a variety of applications in the areas of next-generation mobiles, industrial ultra-high speed image recognition, industrial robot vision, microscope image analysis, video signal processing, 3D stereo vision (e.g., human body measurement and in-vehicle stereo camera), projector-camera system, computational photography, medical image analysis, etc. In particular, we study image registration algorithm, gesture recognition algorithm and high-speed image processing algorithm on embedded processors using 2D/3D-fused visual information.



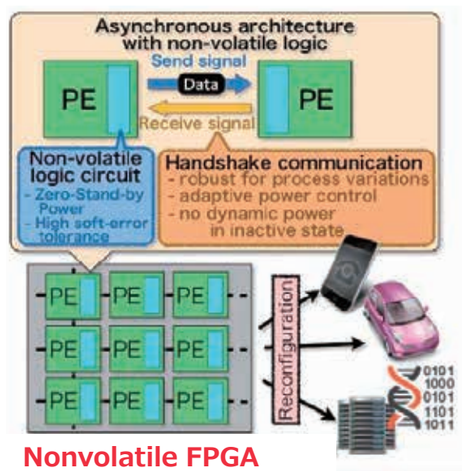
Applications of 2D/3D-fused visual information processing

A Industry – Academic Collaboration Spintronics System Technology

R&D of a VLSI platform for real-world intelligent integrated systems

Prof.
Tetsuo Endoh

The aim of our project is to develop a new reconfigurable LSI with low power, high performance and high soft-error tolerance for real-world intelligent systems, big-data applications and infrastructure applications. For state-of-art process technologies with smaller feature sizes, 3-D integration and an ultra low supply voltage, we develop synchronous/asynchronous hybrid circuits with autonomous supply-voltage control, MRAM-based non-volatile logic circuits for low stand-by leakage power and high soft-error tolerance, and high-level design tools that allow us to exploit easily reconfigurable LSI applications using these advanced circuit technologies.



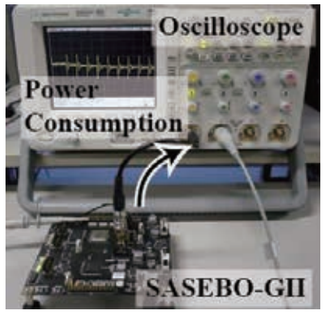
Computer architecture by ultra-low-power reconfigurable LSI (FPGA) based on non-volatile logic with fine-grain power-control capability

A Industry – Academic Collaboration Spintronics System Technology

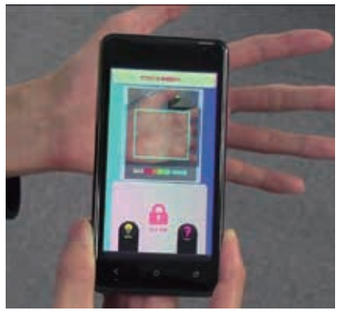
Research and development on embedded security technology

Prof.
Takafumi Aoki

This R&D project aims to study emerging security technologies for IoT (Internet of Things) where numerous and various devices are connected to network. In particular, we study device security and remote authentication technologies for M2M (machine-to-machine) communication. The study for device security includes implementation technologies of confidential communication and authentication under limited resource and power supply. In contrast, the study for remote authentication includes efficient entity authentication technologies between terminal(s) and server(s)/terminal(s). By the above studies, we expect to establish fundamental technologies for connecting various devices in a safe manner to the cyber space.



Implementation security evaluation for M2M devices



Prototype application of remote authentication between terminal and server

A Industry – Academic Collaboration AI Hardware Circuit Technology

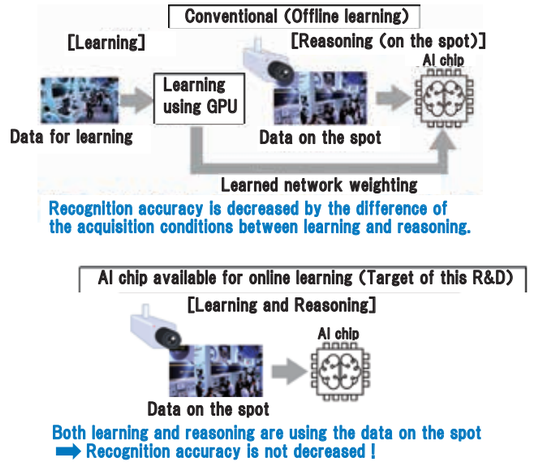
R&D of brain-type processing circuit technologies

Prof.
Tetsuo Endoh

In this research and development, we have developed edge AI processors with low power consumption and high speed which are important for Society5.0.

In the conventional edge AI processors, after learning process which has been performed offline using GPU, learned parameter data have been used for inference process of AI chip. Generally, since the data acquisition conditions at inference (on the spot) are different with those at learning, the recognition accuracy of AI chip is always decreased.

In order to solve this problem, we have researched and developed the architecture / circuit / device technologies of the high-accuracy and ultra-high-speed edge AI processors which can learn and make an inference on the spot. MRAM attracts attention as nonvolatile memory, so we establish a base in the architectures / circuits to utilize MRAM thoroughly, and continue to develop the system-level fine-grain power gating, the high efficiency data transfer mechanism to dissolve data transfer bottleneck, the circuits / devices of MRAM suitable for uses, and the novel AI processor architectures with offline/online learning.



A Industry – Academic Collaboration AI Hardware Circuit Technology

R&D of error correction technologies in flexible information processing


Prof.
Tetsuo Endoh


Specially Appointed
Visiting Prof.
Etsuo Fukuda

In DRAMs and other storage devices, cosmic rays, temperature conditions, and other factors can cause the storage bits to flip, resulting in incorrect calculation results. ECC (Error Correction Code) technology has been developed to detect and correct these errors, by converting the original data into an error correction code with redundancy, which can detect errors and restore the original data. However, in order to increase the correction capability (i.e., to detect and correct more errors), a large amount of redundancy is required to match the capability (Fig. 1).

ECC technology is also used in “memory”, an important component in computers, and in particular, memory that has an ECC circuit implemented as hardware is called ECC memory (Fig.2). Normally, the ECC algorithm called "SECDED", which is capable of correcting 1-bit errors and detecting 2-bit errors, has been commonly used in ECC memory. In this study, we have been exploring and verifying not only SECDED, but also the most suitable ECC algorithm with high correction capability for STT-MRAM based on software, which is easy to implement and improve by trial and error. The BCH code can select the number of bits that can be corrected under certain constraints. On the other hand, Golay codes can detect and correct errors and recover data with a simpler calculation than BCH codes, although the code length and the number of correctable bits are fixed.

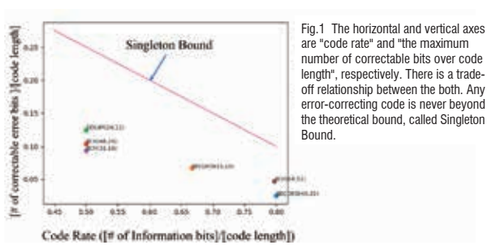


Fig.1 The horizontal and vertical axes are "code rate" and "the maximum number of correctable bits over code length", respectively. There is a trade-off relationship between the both. Any error-correcting code is never beyond the theoretical bound, called Singleton Bound.

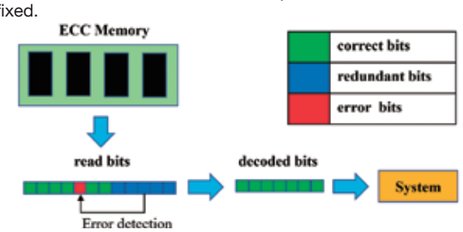


Fig. 2 A schematic figure of ECC Memory. The device can correct error bits in data and send the right data to the system, thanks to redundant bits included within the data.

A Industry – Academic Collaboration AI Hardware Circuit Technology

R&D of MTJ/CMOS Hybrid AI application processors


Prof.
Tetsuo Endoh


Specially Appointed
Visiting Prof.
Etsuo Fukuda

In recent years, advances in Deep Learning (DL) technology have made it possible to recognize objects with high accuracy and high-speed using parallel processors such as GPU, which was previously difficult (Fig.1). While being capable of high-speed computing, those processors consume a lot of power, making them difficult to install in automotive computers and mobile devices.

Most of the power consumption of these processors occurs when accessing memory circuits, and the implementation of the DL algorithm (DLA) in MTJ/CMOS hybrid circuit technology is a promising way to solve this problem. MTJ/CMOS hybrid circuits can reduce power consumption during access to the memory circuit by utilizing the non-volatility of the memory circuit and performing appropriate power gating (PG).

However, existing DLAs are not designed for PG and may not reduce power as much as expected. At present, it is not clear which DLAs are suitable for MTJ/CMOS hybrid circuit technology, and DLAs will need to be improved. Therefore, we are developing a scheme to deploy DLAs on CPU/GPU/FPGA and analyze their performance. (Fig.2). With this scheme, we aim to select and improve algorithms that are appropriate for MTJ/CMOS hybrid circuit technology.

Fig.1 Object detection results recognized by one of famous algorithms, YOLOv3. The algorithm can detect small objects in the picture.

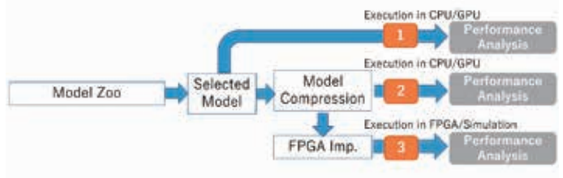


Fig. 2 A scheme of performance analysis of DL model selected from Model Zoo, being executed on CPU/GPU/FPGA. The analysis includes detection accuracy, speed and memory performance analysis, though which we try to select suitable DL models, and modify algorithm of those as well.

A Industry – Academic Collaboration Power Electronics Device Technology

R&D of GaN on Si power device technologies


Prof.
Tetsuo Endoh

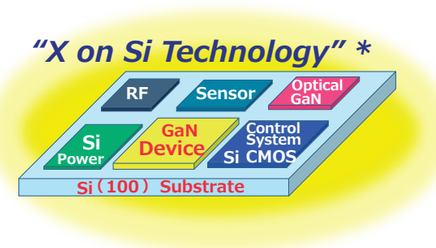

Prof.
Yoshikazu Takahashi


Prof.
Tetsuya Suemitsu

Wide-bandgap materials such as SiC and GaN are paid much attentions as materials of next-generation power devices. Particularly, GaN has already been applied successfully to blue and white LEDs and now is being applied to high-frequency and high-power electron devices. Additionally, GaN is able to be grown on various kinds of substrates including sapphire, SiC and Si. Thus it has a possibility of heterogenous integration with other semiconductor devices.

The goal of this study is, therefore, to build a monolithic integration of GaN power devices with Si devices such as CMOS logic, sensor, RF frontend and so on, on commonly-used Si substrates. This ‘Gan on Si systems’ enable us to downsize the systems dramatically in comparison to the systems combining Si ICs and discrete GaN power devices. Moreover, enhanced performances and their reliability are also expected by reducing interconnections between each device in a module.

The Gan on Si power device systems will be a must-have technology in the future society implementing an intelligent transportation system with a high volume of EV/HV vehicles.



- Bonding-less for high reliability
- Increased functionality
- Enhanced I/O
- Compact size

Advantages of GaN on Si Power device Technology

A Industry – Academic Collaboration Power Electronics Module Technology

R&D of GaN on Si power module technologies

In this research theme, industry and academia are collaborating to develop modularization technology to take advantage of the features of GaN on Si lateral power devices that have both low loss and high speed. This will contribute to EVs and autonomous driving, expansion of data centers, and the realization of smart cities that optimally operate their power supply.


Prof.
Tetsuo Endoh

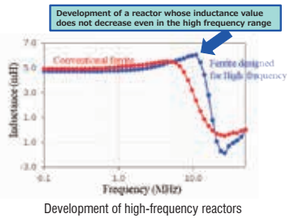

Prof.
Yoshikazu Takahashi

R&D of next-generation electrical component technologies

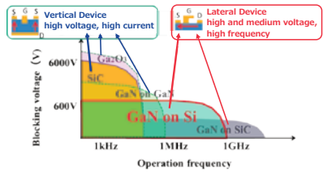
In this research theme, industry and academia are researching and developing DC-DC converters using GaN on Si lateral power devices that can be driven at high frequencies. This contributes to the realization of a highly efficient and ultra-compact DC-DC converter that can handle the increased power supply due to the increase in the number of sensors and actuators associated with the progress of automated driving in automobiles.

R&D of integration and packaging technologies

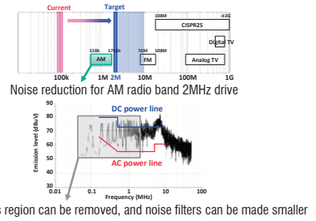
In this research theme, industry and academia collaborate on research and development of assembly integration technologies to take advantage of the superior characteristics of new WBG devices such as GaN-on-Si and SiC. This contributes to reducing the size, weight, functionality, and performance of power electronics equipment.



Development of high-frequency reactors

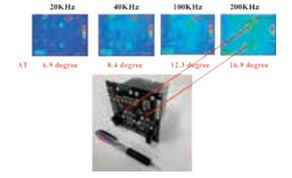


Relationship between blocking voltage and operating frequency of WBG devices



Noise reduction for AM radio band 2MHz drive

Noise in this region can be removed, and noise filters can be made smaller



Suppression of chip temperature rise during high frequency operation of GaN on Si Devices by high heat dissipation layout technology

A Industry – Academic Collaboration | Power Electronics | Circuit Technology

R&D of next-generation high-power converters for power and industry

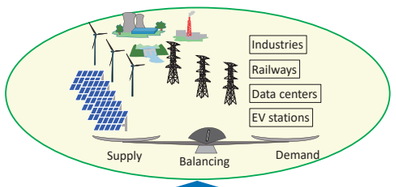
Prof.
Tetsuo Endoh

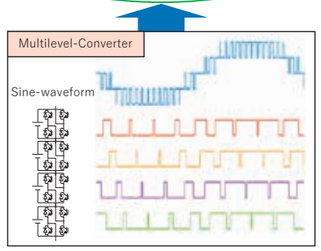
Associate Prof.
Shuji Katoh

In this R & D, with a view to contributing to the mass introduction of renewable energy and electrification, we are developing circuits and control technologies for high-power converters. The converters are for
1) PCSs for wind power generation and solar power generation, etc.
2) The various power equipment installed in factories, large construction machines, ships and EVs etc.

Power converters can be increased in output power by connecting multiple small converters cascaded in series using multi-level technology. Such multi-level converters can output sine-wave voltages with low.

Specifically, the following technologies have been being developed.
(i) Circuit and control technologies to significantly reduce the size of multi-level converters
(ii) Circuit and control technologies to improve the robustness of multi-level converters





B National Project | NEDO | Project for Research and Development of Enhanced Infrastructures for Post 5G Information and Communications Systems

Feasibility study /

Research and development of microfabrication core technologies for nonvolatile MRAM at 1.5nm node and beyond

R&D Director (TEL)
Takashi Hayakawa

Prof.
Shoji Ikeda

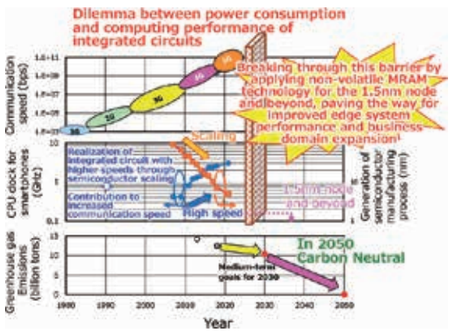
In order to achieve low latency in the post-5G era for edge-side systems such as smartphones and IoT/AI processors, high performance edge computing is necessary under the power supply limitation environment. However, the dilemma of power consumption and computing performance will continue to be an issue in the development of technologies beyond the 1.5nm node, which is an extension of conventional silicon technologies. As a result, there will be limitations in advancing the performance of edge systems and expanding their business fields.

In this theme, research and development of microfabrication technology for nonvolatile MRAM at the 1.5nm node and beyond will contribute to overcoming the dilemma between power consumption and computing performance by reducing power consumption through nonvolatility and miniaturization based on MRAM/CMOS hybrid LSI technology. This will enable the realization of edge-side systems with low power consumption and low latency for the post-5G era, and contribute to carbon neutrality as a synergistic effect of its social implementation.

Based on the following, we will develop fundamental microfabrication technologies for nonvolatile MRAM for the semiconductor process 1.5nm node and beyond;

Tokyo Electron Limited (TEL): Development of core technology for RIE etching at MTJ pitch for the 1.5nm node and beyond

Tohoku University, CIES: Processes development, fabrication, and evaluation to verify the developed RIE technology

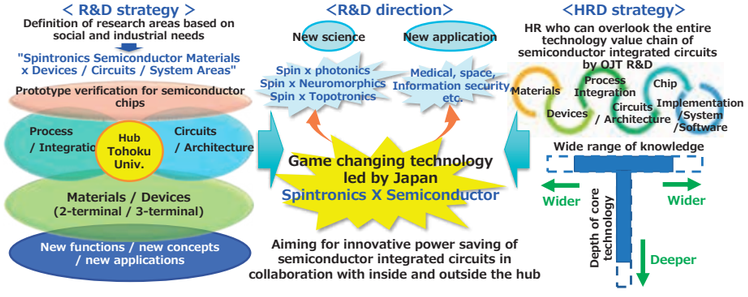


B National Project | MEXT | Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)

Innovative Spintronics X Semiconductor Research Hub

CTO (PSI)
Tetsuo Endoh

We will put spintronics, which is a game change technology for power saving of integrated circuits led by Japan, at the core. We will comprehensively conduct from R&D of new materials and devices, R&D of circuits, architectures and integrated technologies that bring out their characteristics, to prototype verification for power-saving semiconductor chips that accelerate the development of CMOS semiconductors with collaborative and cooperating organizations. While promoting this activity, we will lead the creation of new science and the transformation of the information society by cultivating the fusion area of electronics with light / neuro / topology, and pioneering new applications such as medical care, space, and information security, and then contribute to the improvement of our research and development capabilities related to semiconductors. We have young researchers and students actively and strategically participate in this hub, and develop human resources who have the practical ability and a bird's-eye view.



Overview of the hub concept

B National Project | NEDO | Leading Research for Discovering R&D Issues

AI chips/next-generation computing that enables high efficiency and high speed processing /

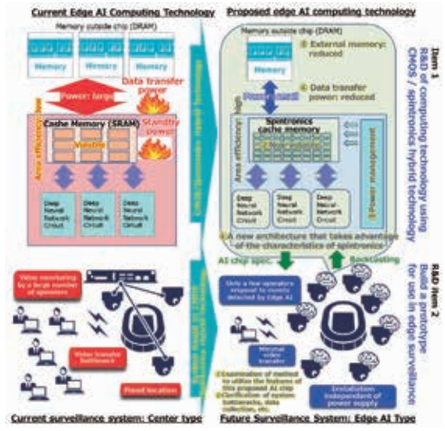
Computing technology using CMOS/spintronics Hybrid technology

Prof.
Tetsuo Endoh

A proposal “Computing Technology using CMOS / Spintronics Hybrid Technology (Representative Institute: Tohoku University, Project leader: Prof. Tetsuo Endoh)” was accepted for “Leading Research for Discovering R&D Issues” in NEDO program “AI Chips / Next-generation Computing that enables High Efficiency and High Speed Processing” in 2021.

The current AI processing has the problem of high power consumption due to high-speed calculation of a large amount of data, and it is necessary to reduce the AI computing power. Especially on the edge side, the permissible power consumption is limited, so innovative power-efficient AI computing technology is desired.

In this research, we will integrate the existing CMOS technology with non-volatile and area-efficient spintronics technology to realize the innovative ultra-low power computing. Then, we will conduct leading research on high power efficiency computing technology suitable for edge AI, and next-generation surveillance systems that will be used as monitoring systems as social implementations.



Overview of this leading research

B National Project NEDO Strategic Innovation Program for Energy Conservation Technologies

Practical application development /

Development of high-speed non-contact AI thermal camera for multi-personnel detection for post COVID-19 hazardous map creation

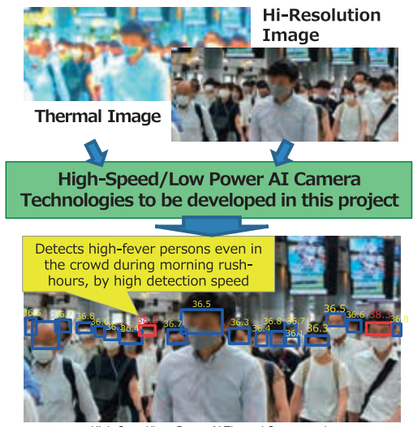

CTO (PSI)
Tetsuo Endoh


Prof.
Shoji Ikeda

The new-type virus infection diseases will come to our community repeatedly. There is inevitable person-to-person contact in our society even after COVID-19. Therefore, we should keep economic activities and daily lives while protecting ourselves from infectious diseases. This approach requires integrating the risk-detecting devices and collected data into cyberspace and visualization of the risks, which will lead to the high-tolerance community against infectious diseases. We thus need the high-speed non-contact AI processor accelerated thermal camera to establish the social innovation as post-COVID-19.

The current thermal camera has a 5~20 persons/sec detecting speed due to the processing power limitation on overlaying thermal and image. This overlay limitation brings that the current thermal camera cannot use for the high traffic area, such as stations in busy time slots, but only for the relatively low traffic locations. It is thus necessary to improve AI microcomputer performance significantly and low power consumption.

This project is developing a high-speed non-contact AI thermal camera for multi-personnel detection with ultra-low power consumption, by utilizing our unique, competitive and innovative AI processor.



High-Speed/Low Power AI Thermal Camera and its High-Speed Temperature Detecting Image

B National Project Tohoku Bureau of Economy, Trade and Industry Strategic Basic Technology Advancement Support Program

Development of spintronics/CMOS Hybrid LSI design technology and software, and their productization


CEO (PSI)
Toru Masaoka

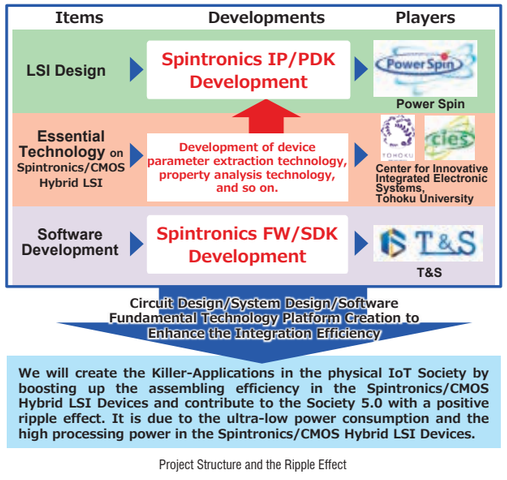

R&D Director (T&S)
Osamu Takamori


Prof.
Shoji Ikeda

Spintronics/CMOS Hybrid LSI Technology that CIES, Tohoku Univ. has been developing to achieve Society5.0 becomes current mainstream to reduce power consumption by 1/100 over the present Silicon CMOS technologies. Therefore, there is a strong demand for the preparation of Process Design Kit (PDK), IP Library, Firmware (FM), and Software Design Kit (SDK) in spintronics/CMOS Hybrid LSI circuit design. They will expand this technology into the application processor with much lower power consumption.

This project consists of three parties. Power Spin Inc. oversees hardware developments. CIES further develops the device parameter extraction technologies, performance analysis and provides to Power Spin. CIES also manages the whole project. T&S inc. develops software such as FM and SDK. These three will work seamlessly to create the concrete foundation of circuit design/system design/speed up the software development.

This project will lead to; 1) ultralow power consumption and improved performance, 2) lower production cost, 3) shorter product cycle time, 4) improved design efficiency and lower design cost, and 5)improved software development efficiency and cost. As a result, Spintronics/CMOS Hybrid LSI Technology can create a new killer application market, a new ripple effect to the other industry, and contribute to the Society5.0 realization.



Project Structure and the Ripple Effect

B National Project JAXA Space Exploration Innovation Hub

Standby power-free system by MTJ/CMOS hybrid technologies and its environmental tolerance test (for space application)


Prof.
Tetsuo Endoh

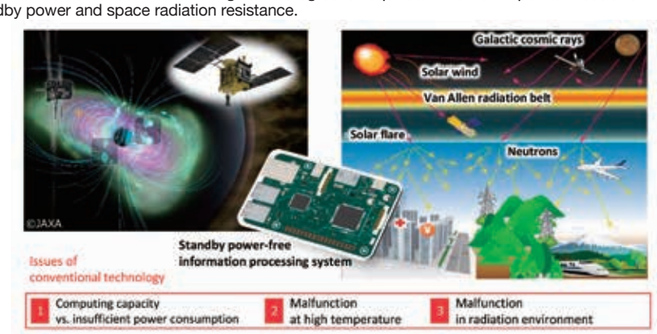

Associate Prof. (JAXA)
Daisuke Kobayashi

A research proposal “Standby-power-free system by MTJ/CMOS hybrid technology and its environmental resistance test (for space applications)” by CIES, Tohoku University in FY2019 was selected for the request for proposal (RFP) by the JAXA Space Exploration Innovation Hub to expand “the human sphere of life and active area by exploring the solar system frontier”. The project was selected as a follow-up research in FY2021, and is accelerating research and development.

For space exploration beyond Moon and Mars, long-term missions of more than 10 years are expected in environments where solar energy is weak, so ultra-low power electronic systems that cannot be achieved with existing technologies is required. Another important issue for spacecraft electronic systems is the need for both standby power and space radiation resistance.

In this proposal, we will research a system that does not require standby power using MTJ/CMOS hybrid technology that integrates CMOS technology and MTJ, which is a spintronic device developed by us. We aim to realize innovative semiconductor devices and integrated circuits that improve efficiency and reduce power consumption by orders of magnitude. Specifically, we will conducted the research on the materials for higher performance and higher reliability, and the MTJ/CMOS hybrid devices/circuits/integration process/chip technologies.

Based on the reliability evaluation including radiation tolerance test by JAXA, we aim to create a power-free integrated circuit that has environmental tolerance in addition to the non-volatility and high speed in MTJ/CMOS hybrid chips. This contributes to the solution of the research theme “Research on Standby Powerless Systems” specified by JAXA.



Research on standby power-free information processing system with radiation tolerance using MTJ/CMOS hybrid technology

B National Project CAO SIP Project (2nd Phase)

CSTI Cross-ministerial Strategic Innovation Promotion Program (SIP) 2nd Phase
“Physical space digital processing platform”
Research sub-theme II. “Ultra low power IoT devices / innovative sensor technologies”

R&D of ultra low power IoT devices and its technical platform with MTJ/CMOS Hybrid technologies for Society 5.0

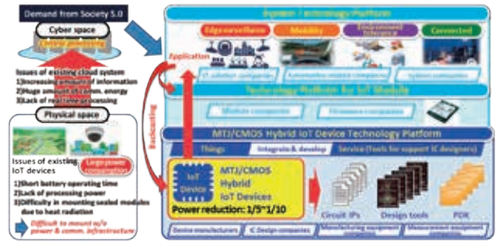

Prof.
Tetsuo Endoh

Tohoku University's proposal ” R&D of ultra low power IoT devices and its technical platform with MTJ/CMOS Hybrid technologies for Society 5.0” (Representative institute: Tohoku University, Project leader: Prof. Tetsuo Endoh) was accepted as a CSTI SIP 2nd Phase “Physical space digital processing platform” Research sub-theme II. “Ultra low power IoT devices / innovative sensor technologies”

In this proposal, using the MTJ / CMOS hybrid technology which has been developed by ImPACT program, the dilemma between the conventional power consumption and processing performance is solved by giving non-volatility (functions that do not forget information even if the power is turned off) in addition to the processing functions to all IoT devices.

In this way, we will establish a platform technology for IoT devices with ultra low power consumption (1/5 - 1/10 compared to conventional) required for physical space. In addition, we have established the technology platform (an integrated system from development and manufacturing to module design) of IoT devices consisting of circuit IPs, design tools, PDK, etc., which are indispensable for IoT device development by defining the application fields: (1) edge surveillance, (2) mobility, (3) environment tolerance, (4) connectivity, in order to implement social implementation of the developed technologies. We also promote cooperation with innovative sensor technology team, common platform technology team, social implementation technology team through development of system technology platform.

This project will contribute that Japan will lead the revolution of innovative low-power IoT devices and the realization of Society 5.0.



Development of IoT devices and it technical platform realizing innovative energy saving performance with MTJ / CMOS hybrid technologies, and system technologies promoting social implementation by backcasting from system development in defined applications.

B National Project JST OPERA Project

World-leading open innovation platform of fusion technologies bridged IT and transportation system areas

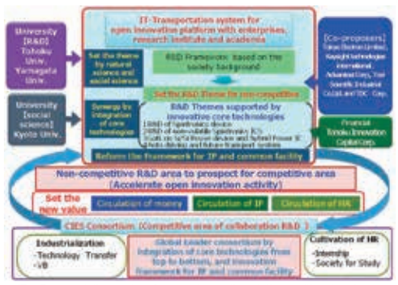
Prof.
Tetsuo Endoh

"World-Leading Open Innovation Platform of Fusion Technologies Bridged IT and Transportation System Areas" proposed by Tohoku University (Organizing institution: Tohoku University; Project leader: Tetsuo Endoh, Director of Center for Innovative Integrated Electronic Systems) was promoted as Program on Open Innovation Platform with Enterprises, Research Institute and Academia (OPERA) in the 2016 fiscal year by JST.

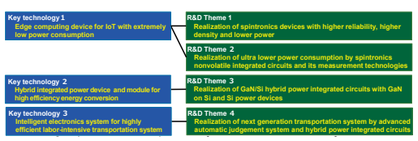
This program works with Kyoto University, Yamagata University, and tens of world-leading enterprises, and aims for creating an open innovation platform about the following R&D areas;

1) Edge computing device for IoT with extremely low power consumption
2) Hybrid integrated power device for high efficiency energy conversion
3) Intelligent electronics system for highly efficient labor-intensive transportation system

We design a non-competitive area for above three R&D areas. We will contribute for the industry to create a new business by the synergy of these non-competitive R&D areas and the competitive one organized by Tohoku University.



IT・Transportation system for open innovation platform with enterprises, research institute, and academia



R&D Themes in National Project of IT・Transportation system for open innovation platform with enterprises, research institute, and academia

B National Project MEXT Research and Development of Basic Technologies for Creating Innovative Power Electronics

Research and development of integrated power electronics for the realization of a decarbonized society

Prof.
Yoshikazu Takahashi

The objective of this research theme is to realize miniaturization, high performance, high power density, and high efficiency of next-generation inverters and power supplies by researching and developing circuit systems that take advantage of the superior performance of WBG devices to the utmost limit and applying optimal passive components.

Applied products include motor drive inverters for EVs, small and medium-sized inverters for industrial use, and power supplies for data centers, which are widely used in society to handle small and medium power ranges.

Tohoku University, which is the representative institution, Ibaraki University and Waseda University, which are research-sharing institutions, and an advisory board as a cooperating company will promote research and development on five sub-themes that are important for power electronics research.

By advancing these research and development efforts, we will create next-generation power electronics technologies and products that will lead the world and contribute to the realization of a decarbonized society.

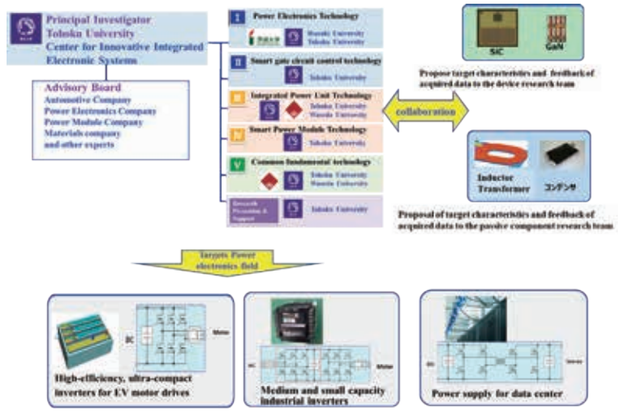


Fig.1 R&D system for integrated power electronics to realize a decarbonized society.

B National Project JSPS Core-to-Core Program

Controlled interfacing of 2D materials for integrated device technology

Prof.
Tetsuo Endoh

Prof.
John Robertson

Prof.
Pierre Seneor

The main objective of this program is to establish the advanced research networks for 2D electronic/spintronic materials with the close collaboration among CIES at Tohoku University, University of Cambridge, CNRS/University of Paris Sud (three core institutes), Engineering Department at Tohoku University, University of Tokyo, University of Tsukuba, Hitachi Cambridge Laboratory, etc. In the networks, we have conducted theoretical/experimental investigation of 2D electron/spin transport in the channel by the development of manufacturing technologies with high-level repeatability for 2D electronic materials using CVD technologies, and high-quality 2D electron/spin channel with high quality interface. In addition to create the breakthrough technologies for the next-generation semiconductor integrated devices, this program also concentrates on fostering young researchers who develop the next generation semiconductor technologies through the collaborations among the above world-class research institutes.

Advanced research networks for 2D electronic/spintronic materials and its members

C J-Innovation HUB

Activities for J-Innovation HUB initiative (International development category)

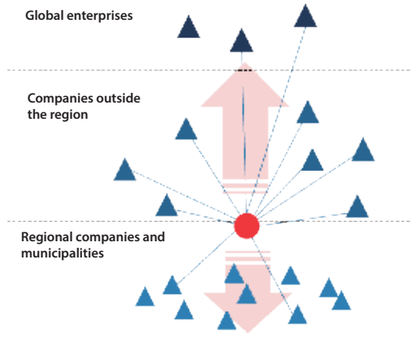
Prof.
Tetsuo Endoh

CIES was selected as the 1st industry-academia base of the "J-Innovation HUB Initiative", a project of the Ministry of Economy, Trade and Industry (METI) launched in 2020 (International development category).

Under this initiative, METI targets regional innovation hubs (mainly universities), and assesses and selects outstanding industry-academia bases that are playing a leading role as hubs for networks of companies. The aim is to enhance their creditworthiness, focus public support measures on them, and enhance the capabilities of the top-ranking hubs. METI selects the hubs in two categories: the international development category and the regional contribution category.

METI will advance dialogues with each of the selected hubs and will provide them with tailor-made support measures, including budgets and relaxation of regulations.

Partners participating in the activities of CIES are expected to take advantage of the preferential treatment of this J-Innovation HUB policy.



International development category Hub

(Source: Ministry of Economy, Trade and Industry)

D Community-based Cooperation Project | Integrated Electronics | Car Electronics

Promotion of regional cooperation in integrated electronics and car electronics fields

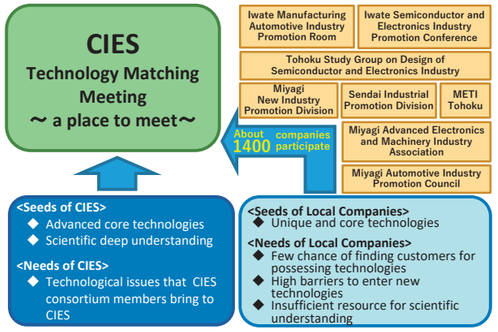
Prof.
Tetsuo Endoh

This activity aims to spread excellent core technologies of local companies to the world with cooperation of local government and administrative agencies. In particular, the following activities have been promoted.

1) Sophisticate core technologies of local companies by integrating fundamental technologies and scientific knowledge of CIES;
2) Develop cooperation among local companies in electronics and automotive field, and apply the core technologies to new application, and work on study meeting of commercialization in cooperation with Miyagi and Iwate Prefectural Government ;
3) Promote cooperation between local companies and world-class companies at CIES as a place to meet, and spread the core technologies of local companies to the world.

Under these activities, unique core technologies by local companies will be applied to integrated electronics and car electronics, and the application and commercialization of the innovative devices will be promoted to next generation of IT and car electronics.

CIES will continue to contribute to Tohoku promotion.



Basic policy of the Community-based cooperation

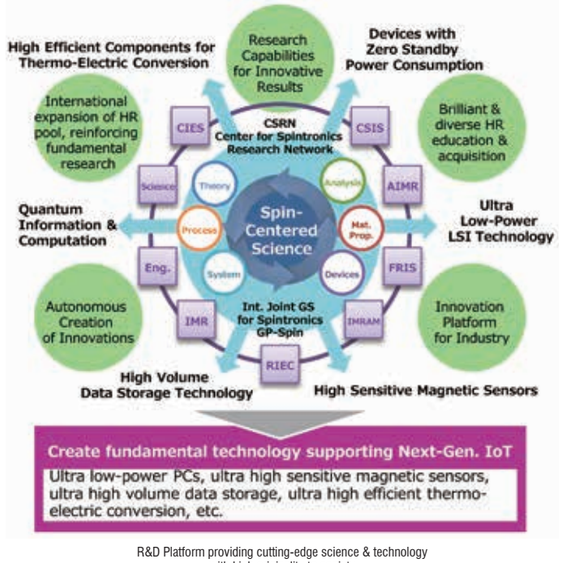
Designated National University | Formation of World Leading Research Center

World Leading Research Center: Spintronics

Tohoku University was designated as “designated national university” from the MEXT in June 2017, which is a national university recognized for its ability and potential for developing the world’s highest level of education and research activities. In the future, it is expected to make a significant contribution to the development of not only Japan but the world.

The university has launched to concentrate the outstanding resources on the high-level research institutes for four areas (① Materials Science, ② Spintronics, ③ Future Medical Care, ④ Disaster Science). In Spintronics area, Center for Science and Innovation in Spintronics (Director: Prof. Yoshiro Hirayama, Deputy-Director: Prof. Tetsuo Endoh) was established from April 2019.

In particular, in the field of spintronics, the university has many distinguished research groups known as the pioneers of the world and has already established itself as a global base. We aim to form a base to strategically integrate outstanding researchers in a wide range of fields from basic to applied through collaborative research with overseas leading universities, and to pioneer the field called “Spin-Centered Science” ahead of the world. Then we plan to create a research and development platform that delivers highly advanced science and technology to society. Here, the university has led the world and “from top science to innovation” by building an international industry-academic collaborative consortium with the CIES as the core, which has been known as Japan’s largest open and closed innovation base.



R&D Platform providing cutting-edge science & technology with high originality to society

Advanced Human Resource Development Program

The following programs have been implemented with the objective of developing young research resources in the field of integrated electronics technology.

① Lectures and curriculum delivered by industry-academia joint faculties (credit courses)

In these courses, we explain the types of talents required in industry sectors and society as a whole, create curriculum based on those principles, and offer lectures by members of industry-academia joint faculties.

② Participating in Tohoku study group on design of semiconductor and electronics industry

We participate in Tohoku study group on design of semiconductor and electronics industry responsible for the human resource development etc. in Tohoku established by Ministry of Economy, Trade and Industry.

③ Industry-academia collaboration OJT system promoting advanced human resource development

●RA system within the consortium

We elucidate the responsibilities of people engaged in industry-academia collaborative research and aim to encourage graduate sudents /postdoctoral / young researchers to participate in industry-academia collaborative research by providing compensation.

●RA System within OPERA Project

We are doing practical human resource development by adding students to industry-academic collaborative research aiming at creating innovative technologies that will become the core of new key industries as Research Assistant (RA).

OPERA Project RA Students

●Internship system

A promotion system has been organized targeting doctoral course students (DCs), post-doctoral fellows(PDs), and young faculties etc., to help to take part in internships at companies participating in CIES consortium.

④ Participating in University program

●Center for Science and Innovation in Spintronics (CSIS)

In the certification of "Designated National University", the CSIS is aiming to establish a hub that pioneers new field of "Spin-Centered Science" in the world by strategically gathering outstanding researchers through international collaborations.

●Center for Spintronics Research Network, Tohoku University (CSRN)

The CSRN is aiming at the formation of research network hub to promote collaborative research with domestic and international institutes for accelerating international competitiveness of world-leading spintronics research, creating new industries, strengthening the current industry and developing next generation human resources.

●Graduate Program in Spintronics, Tohoku University (GP-Spin)

This program aims to foster researchers who can play an active role internationally in spintronics area which is our strength research field. This program is supervised by world leading professors including CIES members.

●Tohoku Forum for Creativity

We participate in a university program that develop human resources who can start a business or play an active role in a company through the research. The program cultivates not only fundamental business skills like management and communication but also advanced skills like setting issues and solving problems.

Strategic Planning Division

Strategic planning division establishes flexible joint research frame work in order to operate it efficiently and actively, based on the world-class core technologies and experienced administration support.

Intellectual Property (IP), which are core IP and emerging new IP, can be managed as our valuable asset and enable to provide them for consortium members efficiently. Based on this new IP system, flexible and global standard joint research contracts are ready for domestic and overseas companies.

Strategic Planning Division

- **Practical IP management** — IP pool / share / acquired sub-systems
- **Contract** — Flexible and global standard
- **Research planning** — Attractive and sustainable topics
- **HR development** — Internship with cooperated companies
- **Publicity** — Public relations for networking

Facility Technology Division

Facility technology division focuses on four main functions in order to achieve safety, stable, and efficient research and development. Not only gas and liquid leakage, particle sensor management, in/out security control for research zone, but also 24 hours monitoring of electricity, gas and water can provide safe and validity research and development circumstance.

We operate a clean room with a 300mm wafer process line. Management duties include daily inspections to ensure stable and safe operations. Maintenance is carried out to ensure stable operation of the 300mm wafer process equipment installed in the clean room.

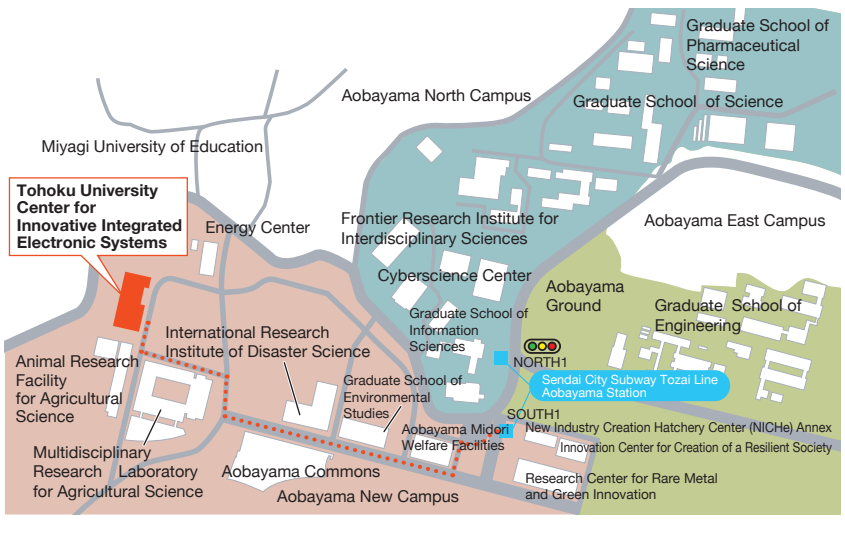
As for ensuring safety, safety education is conducted to the facility and equipment users. To provide instruction and improve safety and health, we established a safety and health committee, safety patrols, and evacuation drills.

As for information security, we manage network security for information equipment in CIES and also provide education to facility and equipment users.

Facility Technology Division

- **Facility management** — 300mm process line / Supply facilities
- **Researche quipment management** — 300mm process equipment / 300mm evaluation tools
- **Safety and health** — Safety and health committee / Safety patrols / Evacuation drills
- **Information security** — Information control / Information leak control / Information security literacy

The center of excellence (COE) of academic-industrial alliance networking the world-wide intelligence and creating new knowledge of humankind by innovative integrated electronics and sophisticated-training-based education



Access

By Subway
Please take subway Tozai Line bound for “Yagiyama Zoological Park Station” from “Sendai Station”, and get off subway at “Aobayama Station”. (about 9 mins ride) Please go out from Exit South 1, and it is about 10 minutes’ walk from “Aobayama Station” to CIES.

Contact

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